

Design and analysis of two stage CMOS operational amplifier using 0.13 μm technology

Abstract

Nowadays, low power operational amplifiers (op-amp) are highly demand for most of the applications such as in medical and communication system. In this project, two stage op-amp is designed and operated at 1.8 V supply voltage. The supply voltage is scaled down to reduce the power dissipation of the op-amp. This is because the power will be high when there is a large supply voltage. The design is simulated and analysed using Mentor Graphic Pyxis software. This two stage op-amp is designed using the Silterra 0.13 μm process technology. The operational amplifier provides a Direct Current (DC) gain of 21.18 dB and a unity gain bandwidth of 6.31 MHz. The gain margin obtained from the op-amp is 14.07 dB and the phase margin of the op-amp is 94.26 ° for 3 pF compensation capacitor and 10 pF load capacitor. The result shows that circuit able to work at 1.8 V power supply voltage and the total power dissipation for the op-amp is 5.35 mW.