IMPLEMENTATION OF FPGA-BASED ARTIFICIAL NEURAL NETWORK FOR CHARACTER RECOGNITION

OMAR SADEQ SALMAN

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IMPLEMENTATION OF FPGA-BASED ARTIFICIAL NEURAL NETWORK FOR CHARACTER RECOGNITION

by

OMAR SADEQ SALMAN
(1332320881)

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TABLE OF CONTENTS

LIST OF TABLE

LIST OF FIGURE

LIST OF ABBREVIATION

ANN	Artificial Neural Networks
ALU	Arithmetic Logic Unit
ASIC	Application-Specific Integrated Circuit
BIST	Built-in Self-Test
BP	Back Propagation
BPNN	Back Propagation Neural Network
CLB	Configurable Logic Block
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
DSP	Digital Signal Processor
FP	Forward Propagation
FPGA	Field Programmable Gate Array
Flopoco	Floating-Point Cores
HDL	Hardware Description Language
IC	Integrated Circuit
IEEE	Institute Of Electrical And Electronic Engineering
IOB	Input Output Block
LCD	Liquid Crystal Display
LFSR	Liner Feed Back Shift Register
LPR	License Plate Recognition

MLP	Multilayer Perceptron
MSE	Mean Squared Error
N_H	Number of perceptrons in the hidden layer
N_I	Number of perceptrons in the input layer
N_O	Number of perceptrons in the output layer
NN	Neural Network
OCR	Optical Character Recognition
PI	Programmable Interconnect
PR	Pattern Recognizer
RR	Relative Risk or Risk Ratio
RTL	Register-Transfer Level
SOM	Self-Organizing Map
SRAM	Static Random Access Memory
VHDL	VHSIC Hardware Description Language
VHSIC	Very-High-Speed Integrated Circuits
VLSI	Very-Large-Scale Integration

Implementation Of FPGA-Based Artificial Neural Network For Character Recognition

ABSTRACT

Artificial Neural Networks (ANN) are non-linear applied math knowledge data modeling tools, usually used model advanced relationships between inputs and outputs or to seek out patterns in data. A generic hardware primarily based ANN is planned and executed using VHDL coding. This project may be seen as a place to begin for learning ANN. It explores in approach a hardware-based application of ANN employs FPGA. The sixteen toggle switches are given as input while the end product is exhibited on the LCD display. This classifier is trained to identify letters on a 4x4 binary grid filled by a user through 16 toggle switches. The most probable class suggested by the ANN is displayed on an LCD screen. To demonstrate the practicality of FPGA execute of ANN, the ANN trained to acknowledge twenty English and nine Arabic character patterns on a 4x4 grid. In structural of ANN, the used of three-layer is implemented entirely with 32-bit single exactitude floating purpose arithmetic to ensure flexibility and accuracy for its wide selection of applications. The resulting design file is programmed into the Altera Cyclone II FPGA on the Altera DE2 development and education board. The design also includes a training supervisor that trains the ANN recognized the total of 29 English and Arabic alphabet predefined characters. The result is promising as the ANN is able to recognize all characters defined to training characters patterns. Each alphabet is tested in 20 English alphabet and 9 Arabic alphabet, after implementation, are done and performance issues of the design are analyzed. The output gives good results, and finally this project shows the flexibility and also the endless chance of hardware primarily based implementation of ANN , the achievement of recognition rate for alphabet English and Arabic character are 76.92% and 32.14% respectively.

Pelaksanaan FPGA Berasaskan Buatan Neural Rangkaian Untuk Watak Pengiktirafanm

Abstrak

Rangkaian neural tiruan (ANN) adalah alat pemodelan pengetahuan matematik bukan linear, kebiasaannya digunakan untuk hubungan model canggih antara masukan dan keluaran atau untuk mencari corak dalam data. Satu perkakasan umum terutamanya berdasarkan ANN dirancang dan dilaksanakan menggunakan kod VHDL . Projek ini boleh dilihat sebagai tempat untuk memulakan pembelajaran ANN. Ia menerokai dalam pendekatan aplikasi perkakasan berasaskan ANN menggunakan FPGA. Enam belas suis togol diberikan sebagai masukan manakala produk akhir dipamerkan pada paparan LCD. Pengkelas ini dilatih untuk mengenalpasti dua puluh huruf bahasa Inggeris dan sembilan huruf bahasa Arab pada grid binari 4x4 yang diisi oleh pengguna melalui 16 suis togol . Kelas paling tinggi kemungkinannya dicadangkan oleh ANN dipaparkan pada skrin LCD. Untuk memperlihatkan praktikal FPGA melaksanakan ANN, ANN dilatih untuk mengakui dua puluh corak huruf bahasa Inggeris dan sembilan corak huruf bahasa Arab pada grid 4x4. Dalam struktur ANN, tiga lapisan dilaksanakan sepenuhnya dengan 32-bit terapung aritmetik ketepatan tunggal bertujuan untuk memastikan fleksibiliti dan ketepatan pilihan aplikasi secara meluas. Fail keputusan rekabentuk diprogramkan ke atas Altera Cyclone II FPGA pada papan pembangunan dan pendidikan Altera DE2. Rekabentuk ini juga termasuk penyelia latihan yang melatih ANN mengiktiraf 29 huruf bahasa Inggeris dan bahasa Arab. Hasilannya amat memuaskan kerana ANN dapat mengenali semua huruf-huruf yang telah ditakrifkan kepada corak-corak huruf latihan. Setiap abjad diuji dalam 20 abjad bahasa Inggeris dan 9 abjad arabic, Selepas pelaksanaan, selesai dan isu-isu prestasi reka bentuk dianalisis. Output yang memberikan keputusan yang baik Secara keseluruhannya, dan akhirnya projek ini menunjukkan fleksibiliti dan pelaksanaan juga peluang yang tidak berkesudahan perkakasan terutamanya berasaskan ANN, pencapaian kadar pengiktirafan untuk abjad Inggeris dan Bahasa Arab adalah watak masing-masing 76,92% dan 32.14%.

CHAPTER 1

INTRODUCTION

The electronic devices production field has witness a great revolution by having the new birth of the extraordinary FPGA family platforms recently. These platforms are the optimum and best choice for the modern digital systems nowdays. The parallel structure of a neural network (NN) makes it potentially fast for the computation of certain tasks. The same feature makes NN well suited for implementation in VLSI technology. Hardware realization of an NN to a large extent depends on the efficient implementation of a single neuron. FPGA-based reconfigurable computing architectures (Ali & Mohammed, 2010) are suitable for hardware implementation of NNs. FPGA realization of ANNs with a large number of neurons (Jung & su Kim, 2007) is still a challenging task.

An ANN is the information processing paradigm that is inspired by the way biological nervous systems, such as the brain and process information. The key element of this paradigm is the novel structure of the information processing system. It is composed of a large number of highly (J. Khan et al., 2001) interconnected processing elements called neurons, working in unison to solve specific problems (Shukla and Kumar (2012)). ANNs, like people, learned by example. An ANN is configured for a specific application, such as pattern recognition or data classification, through a learning process. Learning in (J. Khan et al., 2001) biological systems involves adjustments to the synaptic connections that exist between the neurones. This is true of ANNs as well.

Optical Character Recognition, usually abbreviated to OCR, is the mechanical or electronic conversion of scanned images of handwritten, typewritten or printed text into machine-encoded text. It is widely used as a form of data entry from some sort of original paper data source, whether documents, sales receipts, mail, or any number of printed records. It is a common method of digitizing printed texts so that they can be electronically searched, stored more compactly, displayed on-line, and used in machine processes such as machine translation, text-to-speech and text mining. OCR is a field of research in pattern recognition and computer vision.

Automated OCR has gained impetus largely due to its application in the fields of computer vision, intelligent text recognition applications and text based decision making systems. The approach taken to solve the OCR problem was based on psychology of the characters as perceived by the humans. Thus the geometrical features of a character (Shrivastava & Sharma, 2012) and its variants were considered for recognition (Lerman, Furuyama, & Nugent, 1977). Later, a Template-matching approach was followed that involved comparing input characters to pre-defined templates. This method recognized characters either as an exact match or no match at all (Chandra & Sudhakar, 1988). It also didn't accommodate effects like tilts and style variations that didn't involve major shape alterations. Another approach, namely recognition using correlation coefficients was based on the cross correlation of input characters or their transforms, with the database templates, so as to accommodate minor differences was used. It introduced false or erroneous recognition among characters very similar in shape, such as 'I' & 'J', 'B' & '8', 'O'and'Q' & '0'. The solution to this problem lies in ANN, a system that can perceive and recognize a character based on its topological features such as shape, symmetry, closed or open areas, and number of pixels. The advantage of such a system is that it can

be trained on ‘samples’ and then can be used to recognize characters having a similar (not exact) feature set. The ANN used in this system gets its inputs in the form of feature vectors. This is to say that every feature or property is separated and assigned a numerical value. The set of these numerical values that can be used to uniquely identify each character is called its vector. Thus, a vector database is utilized to train the network, so as to enable it to effectively recognize each character based on its topological properties.

An FPGA is one of the technologies which is getting much attention in recent field of research when it comes to parallel processing. FPGA is a programmable device on which can be developed almost any digital system that using HDL. Since it is programmable and many convenient HDL languages have been developed, engineers tend to use it for their prototype designs before going into ASIC. In this project, the development of recognizing optical characters was performed on hardware using Altera Cyclone II EP2C35F672C6 FPGA chip. A satisfying analysis result of the hardware has demonstrated that the character recognition project using ANN approach shown very promising.

1.1 Problem Statement

The ANN has been widely implemented, however, the current implementations of ANN is mostly software based. This limits the actual capabilities of the ANN as the actual processing is done by the conventional general-purpose processor of the computer system of which the ANN is running on. Even though the ANN had been implemented in hardware before, the total number of hardware based implementations of ANN is limited as compared to the software based implementations. This is because of the complexity of

the ANN itself and the complexity of the resulting circuit when the ANN is to be constructed using hardware devices. The complexity is coming from the structure of the ANN that is depended on three main element, this elements are:

- The structure of the nodes.
- The topology of the network.
- The learning algorithm used to find the weights of the network

For practicality because of this construction, it is more ideal for the ANN to be constructed on a single chip. This again posed another problem as the development of application specific integrated circuit (ASIC) is extremely costly.

Hardware implementation of ANN using ASIC faced another issue due to the high cost that came from the development of the complex ANN circuit, the process to produce the IC, and the lack of demand for ASIC based ANN devices. Furthermore, ASIC based ANN is application specific and cannot be reconfigured for other purposes. This is where FPGA based implementation of ANN comes into perspective. Previously, the FPGA was not seriously considered as the hardware base for implementation of ANN mainly due to its poor performance in yesteryears, but the advancement in FPGA technologies nowadays made ANN implementation on FPGA possible. Moreover, despite the FPGA has considerably inferior performance than ASIC, the flexibility offered by FPGA made it better choice for small-scale implementation of ANN, and it is also possible to reconfigure the FPGA according to the ANN to be implemented.

1.2 Objectives

This project is aimed to acknowledge the character recognition ANN approach on hardware-based FPGA. This contain the fundamental purposeful structure and style of ANN, the algorithms to run the ANN and conjointly (training and educational) rules to training the ANN to produce the expected result. The main objectives of this project is to implement the FPGA primarily based ANN for character recognition application and to be prepared acknowledge type of characters to match the output from the ANN with the actual result.

1.3 Scopes

The research focusing on improving the system performance of the character recognition ANN approach using FPGA, and explain the architecture for ANN implemented on FPGA board. These included learning algorithm to train the ANN system using feed forward (FF) and back probagation (BP) algorithms. An analysis the classification of training and accuracy of analysis cost and effeciencies.The resulting data obtained from the deployment of the ANN is collected and analyzed. Data analysis is presented to be used by others in a format and easily understood by other reader. Moreover, the illustrate the advantage of this system to people in the life.

1.4 Contribution of the Research

This analysis will introduce a new hardware based totally implementation of ANN and to preface a brand new FPGA style for implementing academic degree ANN to

undertake to cut back the price and power consumption, the implementation of ANN on hardware as in FPGA is anticipated to beat the slower method speed of current package primarily based mostly implementation of ANN, i.e. character recognition. That associate with these systems have driven researchers to seem for appropriate platforms.

1.5 Thesis Organization

This thesis will cover the project of FPGA implementation of ANN for character recognition. It is organised as follows:-

- Chapter 2 will introduce the structure of biological neuron, the basic of ANN and its learning algorithm, the HDL used in this project, and the FPGA. This chapter also explore the related works regarding this project and the tools used throughout the project.
- Chapter 3 discusses the proposed methodology and how to implemented this system on the FPGA DE2 board. It will explain the steps taken to implement the ANN on FPGA device and to apply the developed ANN for character recognition.
- Chapter 4 demonstrates the result of the system and explain the number of character using in this work.
- Chapter 5 concludes the whole project and provides a few things that can be improved concerning the project in the future.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Bio-inspired ideas such as NNs, evolution and learning have attracted abundant attention. Recently, a result of growing interest in the automatic design of advanced and intelligent systems that result in adaptation and fault tolerance. Engineers and computer scientists have studied these biological concepts in an effort to replicate their desired qualities (Hanan A. R. Akkar & Mahdi, 2010) in computing systems. The necessities for advanced integration, intensive on board process, and low power consumption, so FPGAs emerge as a technology of alternative that strikes the best balance between process power, energy necessities, and flexibility , through the power of reconfigurability (Khammas, 2012).

The conception of ANNs is emerged from the principles of brain that translated to digital computers. In 2007, this is the first works of ANNs were the models of neurons in brain arithmetic rule by Haykin (Haykin, 2007). These works show that neuron in ANNs take some data as associate number of input from associate degree other neuron or from an external input. This data is propagated as associate degree output that computed as weighted add of inputs and applied as non-linear perform.

Architectural ANNs parameters such as numeral of inputs per neuron and every neuron's conduction variation remarkably from one application to another.

Thus, for special purpose network architectures parameters should be neatly balanced for effective implementation (Sahin, Becerikli, & Yazici, 2006).

FPGA is a sort of programmable logic, which provide flexibility in style like software system, however with performance speeds nearer to Application specific integrated circuits (ASICs), NN implementation in hardware employ FPGAs are chosen for implementation ANNs with the following reasons (Khammas, 2012).

- They can be applied a wide range of logic gates starting with tens of thousands up to few millions gates.
- They can be reconfigured to change logic function while resident in the system.
- FPGAs have short design cycle that leads to fairly inexpensive logic design.
- FPGAs have parallelism in their nature. Thus, they have parallel computing environment and allows logic cycle design to work parallel.
- They have powerful design, programming and syntheses tools.

Until recently, the sole alternatives were to develop custom hardware (typically board level or ASIC), buy expensive fixed function processors, or use associate degree array of microprocessors. FPGAs provide a chance to accelerate your digital signal process application up to a thousand times over a conventional DSP chip. The most goal here is coming up with associate degree OCR system in FPGA and to develop algorithms that are appropriate for hardware implementation of OCR. The applying projected here is automatic activity of instrument supported OCR system in FPGA. This solution benefits from significant reducing of work quantity for calibration as well as from better