

Design of 3.1-10.6 GHz UWB CMOS Power Amplifier using Cascade Topology

Abstract

Power amplifier is an important component in the wireless communication system. Design of the power amplifier in UWB transceiver is challenging as the signal need to be transmitted over a wide bandwidth. Several criteria need to be fulfilled such as good linearity, good wideband matching, high efficiency and low power consumption. This paper presents the design of a power amplifier with 3.1-10.6 GHz using 0.18 μm CMOS technology for ultra-wide band application. The proposed power amplifier used three cascaded amplifier stages in order to achieve good gain and wide-band width. The results show that the proposed power amplifier design has an average gain of 7.28 dB, an input return loss less than -7.48 dB, an output return loss less than -4.782 dB, and group delay variation of ± 151.9 ps is achieved over the entire band. A good input 1dB-compression point of 6.67 dBm and input third order intercept point of 0 dBm is achieved at 5 GHz.

Keywords

CMOS; power amplifier; Ultra-wideband cascade topology