HARDWARE IMPLEMENTATION OF RGB TO HSL CONVERTER USING FPGA

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by

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In the name of God, Most Gracious, Most Merciful

Dedicated to

My beloved parent

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LIST OF ABBREVIATIONS

CCTV	Closed Circuit TV
RGB	Red, Green, Blue
HSL	Hue, Saturation, Luminance
HSV	Hue, Saturation, Value
YCbCr	Y(luma), Cb(Chroma Blue), Cr(Chroma Red)
FPGA	Field Programmable Gate Array
VGA	Video Graphics Array
VHDL	VHSIC (Very High Speed Integrated Circuit) Hardware
HSI	Hue, Saturation, Intensity
ROM	Read Only Memory
VLSI	Very Large Scale Integration

PERLAKSANAAN PERKAKASAN UNTUK PENUKARAN RGB KE HSL MENGGUNAKAN FPGA

ABSTRAK

Model warna RGB (Merah, Hijau, Biru) adalah asas kepada model warna dan dicantumkan bersama untuk menghasilkan julat warna penuh. RGB tidak dapat menghasilkan maklumat yang mencukupi untuk menganalisa imej digital. HSL (Hue, Saturation, and Luminance) adalah model warna lain untuk RGB. HSL berkebolehan untuk menyediakan maklumat yang boleh digunakan sepenuhnya seperti sudut warna, ketepuan warna dan kecerahan warna. Maklumat ini digunakan sepenuhnya untuk menganalisis imej. Dalam kerja ini, perlaksanaan algoritma penukaran matematik RGB ke HSL menggunakan bahasa VHDL. FPGA membolehkan keupayaan keselarian untuk mempercepatkan proses penukaran daripada langkah-langkah memproses dan hanya menggunakan satu kitaran sahaja. Persamaan RGB ke HSL dilaksanakan dengan menggunakan dua kaedah iaitu senibina '*parallel*' dan '*7-stages pipeline'* dengan menggunakan bahasa VHDL. Senibina '*parallel'* hanya mempunyai satu tempoh masa kelengahan data. Kedua-dua kaedah ini boleh menghasilkan nilai HSL bagi setiap pixel tanpa kelengahan data daripada 10Hz hingga 150MHz. Senibina-senibina *'parallel'* dan *'pipeline'* untuk penukar RGB ke HSL telah mencapai ketepatan dengan pengesahan perkakasan masing-masing sehingga 99% dan 98%.

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ABSTRACT

The RGB (Red, Green, Blue) colour model is the basic colour model and add together to produce full colour range. RGB is unable to produce sufficient information for digital image analysis. The HSL (Hue, Saturation, and Luminance) is another colour model for RGB. HSL is capable to provide other useful information such as colour in degree, saturation of the colour and brightness of colour. These information are useful for image analysis. In this work, the implementation of RGB to HSL mathematic conversion algorithm in FPGA is using VHDL language. FPGA enables parallelism and pipelining capabilities to speed up conversion process of the processing steps and consumes only one cycle. The RGB to HSL equation is implemented by using two methods which are parallel and 7-stages pipeline architectures using VHDL language. Parallel architecture has only one clock period of data latency. These two methods can produce HSL value for each pixel without data latency from 10Hz to 150MHz. The parallel and pipeline architectures for RGB to HSL converter have achieved rate of accuracy with the hardware verification up to 99% and 98%, respectively.

CHAPTER 1

INTRODUCTION

1.1 Introduction

Nowadays digital image is the most popular image form in the world. With its highly portable capability, mathematical operation friendly and small memory storage size has caused digital image to empower the imaging technology in the world. The digital image can be produced by digital camera and close circuit television (CCTV). The pixel colour in digital image is represented by several colour spaces such as Red-Green-Blue (RGB), Hue-Saturation-Luminance (HSL), Hue-Saturation-Value (HSV), Hue-Saturation-Intensity (HSI), and Luma-Chroma (YCbCr).

Each colour model has its specific application and features. RGB colour space is one of the most common use colour space in digital image. This is because RGB colour space is simple and compatible with binary machine. Some application of digital image required to use other colour space for processing such as HSL space. HSL colour space is a popular space used in machine vision technology for object recognition process. Many of the object recognition process are developed base on object colour recognition to detect the target. Therefore the HSL space used to enhance the image colour during image processing on the image. Hue is the colour plane of the RGB, saturation is the colour intensity of the RGB in the image and video while luminance is the colour brightness of the RGB.

By using Altera FPGA DE2 board as hardware platform, it helps to increase the conversion yield. RGB to HSL conversion algorithm are implemented using software and

hardware languages. The VHDL is in order to simplify the conversion steps and speed up the process.

1.2 Problem Statement

Currently, there are many existing RGB to HSL converter method used in image processing available but most of them are based on software. The problem with the software is that its implementation is not suitable in practically used if compared to hardware based. It consumes multiple clock cycle to complete 1 operation. Besides, the RGB colour model is an additive colour model in which red, green, and blue light are added together in numerous ways to reproduce a broad array of colours but there is limitation for RGB colour model to provide sufficient information for image analysis. HSL is a colour model that different from RGB. HSL provides the information such as colour in degree, the saturation of the colour and the brightness of the colour. This information is much more suitable for image analysis. Parallelism and pipelining capabilities of FPGA has simplified the processing steps and only consumes one clock cycles to produce the HSL value for each pixel without data latency. Hence, the embedded FPGA-based RGB to HSL converter with less computational time and capable to work on images analysis should be developed.

1.3 Objectives

The main objective of this research project is to fully implement RGB to HSL hardware FPGA-based converter. In order to do that there are few steps need to be taken. These include

i. to develop of parallelism and pipeline architectures of RGB to HSL hardware converter.

ii. to analyse hardware conversion output accuracy for both converter as well as characterizing the implementation issues that limit the achievable throughput.

iii. to investigate and analysis a maximum operation frequency for both converter to achieve a high performance, evaluating the interaction between algorithm and hardware efficiency to determine which variants are most suitable for hardware implementation.

iv. to compare hardware resources usage for both converter.

1.4 Scope of Works

This research is bound to the following scopes:

i. The selection of a formula used RGB to HSL conversion and development of C code and VHDL for it.

ii. Using a serial RS232 to collect data in text file and interfacing a CCTV and VGA to the Altera FPGA DE2 Board.

iii. Implementing simulation and applied on the FPGA hardware board as well as capturing the image into SD card for analysis and performance.

iv. Performances measurement is evaluated in terms of frequency used and percentage of accuracy rate.

1.5 Thesis Organization

This thesis consists of 5 chapters as following:

Chapter 1 briefly introduces about digital images and how it's represented by several colour spaces such as RGB, HSL, HSV and YCbCr. The explanation of FPGA and how it works is also presented. Problem statement, objectives, and scope of work are stated clearly.

Chapter 2 conducts a review to previous works. It also covers the theories and conversion of RGB to HSL converter. Besides, an explanation on the application, implementation platform and method of implementation on hardware architecture also presented.

Chapter 3 describes the methodology of coding and hardware implementing in the Altera FPGA DE2 Board. This covers the work from software development, hardware implementation and hardware real time performance. The details of hardware conversion architectures are also mentioned in this chapter

Chapter 4 presents the results and discussions based on designing VHDL code in the board by using Altera Quartus II software and data analysis on the image results. It also demonstrates the stages of pipelining architecture and performances of testing architecture.

Chapter 5 summarizes about the findings, conclusions and future work recommendations for the RGB to HSL converter. Following these are the lists of references, and sample of programming and some testing data/results.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter discusses the theories and principles of Hue, Saturation, and Luminance (HSL) colour space. It also reviews some of the related work in related field and includes the concept, implementation platform, design structure, and applications of the HSL colour space.

2.2 Field Programmable Gate Array (FPGA)

FPGA is a type of semiconductor device that contain programmable logic and interconnections which mostly used in logic or digital electronic circuits. The programmable logic components or logic blocks as they are known may consist of anything from logic gates, through to memory elements or blocks of memories, or almost any element. FPGA supports thousands of gates and popular for prototyping integrated circuit (IC) designs. Once a design is set, hardwired chips will be produced to faster performance. FPGA chip is programmable and reprogrammable which is considered as an advantage of it. In this way, it becomes a large logic circuit that can be configured according to a design, but if changes are required it can be reprogrammed with an update. FPGA contains many identical logic cells that can be viewed as standard components. Each design is

implemented by specifying the simple logic function for each cell and selectivity closing the switches in the interconnect matrix. The array logic cells and interconnects form a basic building blocks for logic circuits. Complex designs are created by combining these basic blocks to create the desired circuit. The logic cell architecture varies between different device families.

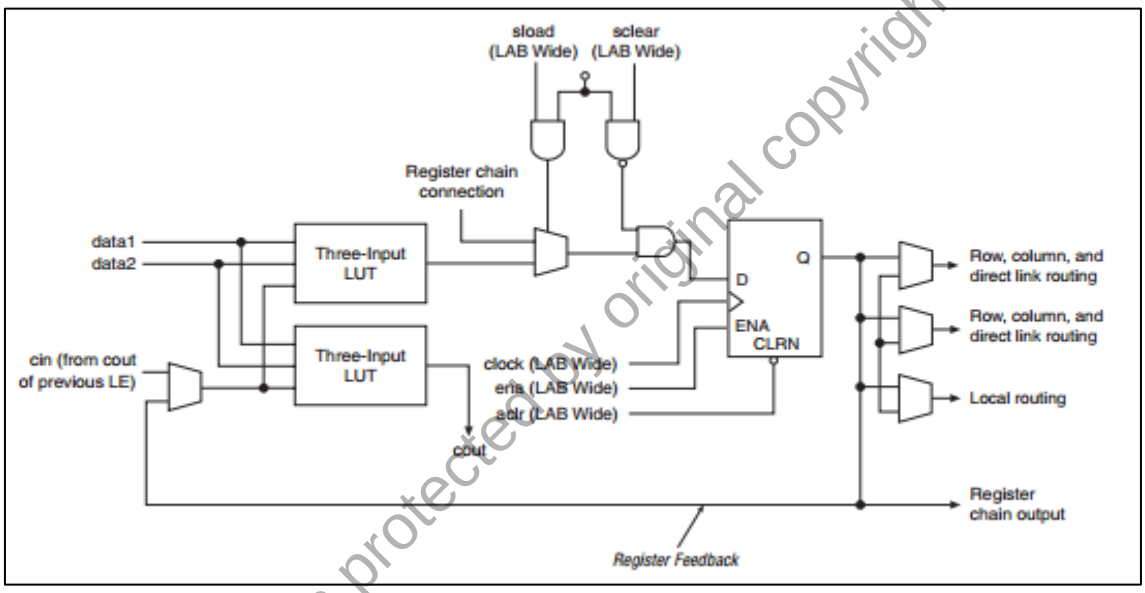

Figure 2.1: Illustration of Logic Cell (Cyclone II Handbook, 2011)

Figure 2.1 shows a simplified illustration of a logic cell. Each logic cell combines few binary inputs to one or two outputs according to a Boolean logic function specified in the user program. In most families, the user also has the option of registering the combinatorial output of the cell, so that clocked logic can be easily implemented. The cells combinatorial may be physically implemented as a small look-up-table (LUT) memory or as a set of multiplexers and gates. LUT devices tend to be a bit more flexible and provide more input cell than multiplexer cells at the expense of propagation delay.