IMPLEMENTATION OF IMAGE PROCESSING FUNCTIONAL UNIT USING SPATIAL PARALLELISM ON FPGA

By

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To my beloved mother and father
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LIST OF ABBREVIATIONS

ASIC	Application Specific Integrated Circuits
DSP	Digital Signal Processing
FPGA	Field Programming Gate Array
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
HDL	Hardware Description Language
DE2	Development and Education
DIP	Digital image processing
GPU	Graphic Processing Unit
SIMD	Single Instruction Multiple Data
API	Application Programming Interfaces
CPU	Central Processing Unit
RAM	Random-Access Memory
SRAM	Static Random Access Memory
ROM	Read-Only Memory
PLD	Programmable Logic Devices
IOB	Input / Output Logic Blocks
CLB	Configurable logic blocks
LUT	Look-Up Table
SOC	System on Chip
TTM	Time to Market
CB	Connection Block

SB	Switch Block
CS-Box	Connection-Switch Box
GRM	General Routing Matrix
GSB	General Switch Box
PLL	Phase-Locked Loop
DLL	Delay-Locked Loop
NCD	Native Circuit Description
MUX	Multiplexer
IDB	Input Data Buffer
ODB	Output Data Buffer
VGA	Video Graphics Array
LCD	liquid-crystal display
RTL	Register Transfer Level
DAC	Digital to Analog Converter
SRAM_OE	SRAM Output Enable
SRAM_WE	SRAM Write Enable
SRAM_LB	SRAM Low-Byte Data Mask
SRAM_UB	SRAM High-Byte Data Mask
SRAM_CE	SRAM Chip Enable
RGB	Red-Green-Blue

Pelaksanaan Unit Fungsian Imej Pemprosesan menggunakan Keselarian Spatial ke atas FPGA

ABSTRAK

Terdapat pelbagai jenis algoritma imej telah digunakan untuk meningkatkan imej dalam domain spatial Pelaksanaan berjujukan telah digunakan dalam pemprosesan imej sebagai pendekatan utama dan perlaksanaan ini memakan banyak masa, kerana imej yang digunakan mempunyai data yang besar untuk diproses. Oleh itu, ianya satu keperluan menggunakan pendekatan selari untuk mempercepatkan pemprosesan imej. Beberapa teknologi telah digunakan untuk menyokong keselarian. Field Programming Gate Array (FPGA) adalah teknologi yang penting dalam menyokong keselarian tepat di samping berpotensi konfigurasi.Projek yang dicadangkan adalah berkenaan dengan reka bentuk dan pelaksanaan algoritma dipilih untuk meningkatkan ciri-ciri imej seperti kontras, kecerahan, ambang, serta songsang.Dalam projek ini, ciri-ciri keselarian yang terdapat dalam FPGA diterokai dengan menggunakan keselarian spatial untuk membina sistem masa nyata terbenam.Perkakasan dan perisian pelaksanaan sistem pemprosesan imej untuk meningkatkan imej skala kelabu pada domain spatial telah dicadangkan.Modul VHDL dan megaCore telah digunakan dalam melaksanakan reka bentuk yang dicadangkan.Penggunaan tenik selari ke atas cip daftar dan memori dapat meningkatkan masa pemprosesan algoritma dilaksanakan.Dalam membina FPGA papan DE2-115 digunakan peneraju utama projek. Keputusan daripada perlaksanaan reka bentuk menunjukkan bahawa throughput itu meningkat dari segi skala coarse-grain. Selain itu, frekuensi pengendalian dipertingkatkan dengan meningkat kepada 1 GHz dengan konfigurasi Phase-Locked Loop (PLL).Tambahan pula, peningkatan imej yang diterima boleh diperolehi dengan menggunakan proses penalaan ke atas algoritma yang dilaksanakan.

Implementation of Image Processing Functional unit using Spatial Parallelism on FPGA

ABSTRACT

There are varieties of image algorithms have been used to enhance images in spatial domain. The sequential implementation was used for image processing as main approach and it consume a lot of time, since images have massive data to process. Therefore, there is a necessity to use parallel approach to speed up image processing. Few technologies are used to support parallelism. Field Programming Gate Array (FPGA) is most significant technology supporting true parallelism in addition to reconfigurability potential. The proposed project is concerned with the design and implementation of selected algorithms to enhance image features such as contrast, brightness, threshold, and invert. In this project, the parallelism features on FPGA is explored by applying spatial parallelism to build embedded real time system. A hardware and software implementation of image processing system to enhance gray-scale image on spatial domain is proposed. The VHDL and megaCore modules are used to implement proposed design. The utilization of parallel on-chip registers and memory enhanced the processing time of implemented algorithms. An FPGA development Board DE2-115 is used as vehicle project. The results of implemented design show that the throughput is increased in term of coarse-grain scale. Also, the operating frequency is increase to 1GHz by configuring Phase-Locked Loop (PLL). Furthermore, an acceptable image enhancement is obtained by applying tuning process on implemented algorithms.

CHAPTER 1

INTRODUCTION

1.1 Overview

Digital image processing has grown dramatically in recent years because of its usage in many applications in different aspects of human modern life. However in many cases, the obtained images are not clear-cut. These applications require performing preprocessing operations to clarify images features such as image enhancement. Different ways and a variety of types of processing to enhance the images have been used. In the early stages, a sequential processing was used for image enhancement. This type of processing consumes a lot of time since the images have a massive data. Thus, it's necessary to use parallel processing to speed up the implementation of operations on the images. Many ways are used for parallel processing using software or hardware. The implementation of applications with specific hardware (embedded system) provides better speed than implementation of applications with specific software (Sharma, Pandy & Khan ,2013).

In hardware technology design, there are two classes: full custom hardware, known as Application Specific Integrated Circuits (ASIC) which its design cannot change, and hardware. Semi-custom hardware design techniques such as parallelism and pipeline can be developed using (FPGA) which is not possible in designing the dedicated (DSP). The FPGA has a good feature such as configurable, low power consumption, work in real-time, minimize the product cost, and able to perform complex algorithms. Due to several reasons, the applications of image processing are suited for implementations on configurable computing hardware (Demler, 2011; Wilson, 2009). This is because many operations of

image processing need only simple logical and arithmetic and operations that are much fitted to configurable hardware (Levine, 1999). As well as the flexibility of modification the implementation from one function to another quickly is using the same hardware Moreover, the parallelism in algorithm could exploit in image processing application with high degree.Since the image operation are used for each pixel in apportion of an image or the whole image, this will lead to a significant increasing in the time consummation for large image processing (Nelson, 2000).

All systems of computing are constructed from interconnected components, such as transistors, gates, registers, arithmetic units, memories, or complete processors. Depending on the level of abstraction at which a system is viewed, at all levels of abstraction there are two fundamental to create parallel computing structures: spatial and temporal parallelism. In-temporal parallelism, the processing function is partitioning into a number of sub-functions. One functional unit exists to carry out each sub function which applied sequentially to each unit of information. The successive units are worked at the same time. While in spatial parallelism, simultaneous execution of tasks is done by using several processing units. These units can execute the same task or different tasks. The parallelism amount in spatial parallelism depends on the number of independent tasks while in temporal parallelism depends on the divisibility of the task parallelized (Gümüşkaya & ÖRENCİK, 1999).

These theses explain the designing and implementing a real-time system on FPGAs. Since FPGAs have distinctive properties that are highly recommended to be used the system design and implementation. To increase the operating frequency by using on-chip PLL (Phase-Locked Loop) is a way to solve the problem related with low operating

frequency. The oscillators in the FPGA testing board that provides three clock signals with 50 MHz only but when use the (PLL) can increase operating frequency up to 1GHZ(Altera, 2010), improve the performance of system parts alongside with real-time response taking advantages of hardware capability, as well as reduce the effect of hardware limitations such as memory and other peripheral device that makes system parts very efficient in terms of time. The FPGAs reconfigurable make them very suitable choice for real-time image processing to implement many enhancement algorithms that need complex computation.

There are two essential hardware design languages that are used to configure: Verilog HDL and Very High Speed Integrated Circuits (VHSIC). The VHDL is hardware description language used to design digital circuits that allows designers to design an application at diverse abstraction levels. Verilog HDL and VHDL are techniques for specialized design that cannot be accessed immediately to software engineers that are workout using imperative programming languages. In the system of this study, the VHDL hardware description language will be used for hardware design. Also, the necessities to achieve better results and performance for their applications. This work provides an implementation of different complex algorithms on FPGA. The implementations make the use of parallel functional unit to invest the parallelism by execution the instructions in parallel in spatial domain. Thus, the implementation will take less time consuming for the enhancement processing. The development and education board (DE2_115) will used to implement the proposed system for image enhancements.

1.2 Problem Statement and Motivation

To overcome data processing delay and fine tuning of process with lower complexity design, the real-time image processing functional unit needs a computational platform that is robust, true parallel, and reconfigurable. In addition, the platform should be structural and scalable.

Currently, image processing platforms are Application Specific Integrated Circuits (ASIC), Digital Signal Processing (DSP), Microprocessor and Embedded soft core processor on FPGA such as Altera NIOS II and Xilinx Microblaze.The major problems confront these platforms are implementation of true parallel application and lack of massive data processing performance because off-chip memory utilization. These platforms are unable to fulfill the whole embedded image processing system requirements for effective and efficient parallelism and fast processing (Pal, Kotal, Samanta, Chakrabarti & Ghosh, 2014).

Researchers resort to post-processing and parallel programing scenarios to overcome the inability problem. Although the post-processing is accurate and effective, this scenario is not applicable for online processing. Also, parallel programing is considered successful approach but still lacking of true parallelism and workload balance of processor resources utilization(Passas, Kotsis, Karlsson & Bilas, 2008). Therefore, to avoid both approaches, a platform that has an efficient spatial parallelism design and high processing power with low level of design abstraction is needed to fulfill the requirement of embedded image processing functional unit.

1.3 Research Objectives

The aim of this project is to implement the processing functional unit which harnessed the principle of the spatial parallelism and obtains the full advantage of the FPGA unique features. In order to achieve this aim, the objectives of this research are:

i. To design and implement embedded real-time system that performs many algorithms by utilizing spatial parallelism approach on FPGA

ii. To increase the operating frequency of processing modules.

iii. To verify and evaluate the design performance of the system by using FPGA CAD tool and on board testing.

1.4 Research Scope

This project produces a suitable hardware for implementing a real-time system for techniques of gray-scale image enhancement that used field programmable gate array (FPGA).The project provides implementations of many algorithms in image enhancement such as contrast stretching, brightness control, threshold and negative transformation, on FPGA that have become competitor substitute for applications in better quality in digital signal processing. These algorithms can be implemented on retinal images successfully in VHDL by using (DE2_115 board). The project goal is to simulate and implement these algorithms using VHDL. The DE2_115 board from Altera is the device that is selected here to implement these algorithms .The functionality of design and timing are verified by performing the simulation using real input images.

1.5 Contribution of the research

The projects contribute to design and implement a hardware system as follows:

I. In this project, the parallelism features on FPGA is explored by applying spatial parallelism to build embedded real time system to perform many techniques to enhance gray-scale images at the same time. Therefore, the throughput is increased in term of coarse-grain scale

II. The operating frequency of processing spatial modules is increase to 1GHz by using (Phase-Locked Loop).

1.6 Thesis Organization

The organization of this thesis includes five chapters as a follow:

Chapter 1 introduces approach on FPGA and some research background. Motivations for research and problem statement are also defined. Goals, objectives and scopes of research are stated. Finally, research contributions are presented.

Chapter 2 introduces the image enhancement. This chapter introduces a briefly related work that was accomplished in this area of parallel computing architectures and the system advantages that make use of spatial parallelism computing in systems design. I also introduce brief knowledge about various aspects that relate to the FPGA applications.

Chapter 3 describes the implementation image enhancement methods to achieve the goal of the project. Moreover, the chapter provides a highlighted overview about the system design and its modules, as well as with each functionality.

Chapter 4 presents the result obtained, discussion and detailed explanation of investigation phase and implementation phase.

Chapter 5 introduces the conclusions derived from the entire implementation of the system. The future work is also discussed in this chapter.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Image processing is considered one of the most rapidly evolving areas of information technology; its applications are used in all fields of knowledge. Digital images often suffer from the poor quality, particularly lack of contrast and presence of shading and artifacts, due to the deficiencies in focusing, lighting and other factors. Due to these reasons, the detectable of these images by eye becomes hardly .It is quite important to do some processing to make images more suitable for a given task and a specific observer, easier for visual interpretation and understanding (Raines, 2004).

Image enhancement is a method which is used to improve image vision and makes the image adapt to be processed by a computer. Processes of image enhancement comprise a collection of techniques to improve the appearance of image visual or the image conversion to a form better suited for analysis by machine or human (Russ, 2015). They work by modifying the image brightness, contrast, or the distribution of the gray levels. The existing image enhancement techniques can be classified into the flowing types: (Point Operation, spatial Operation, and Transform Operation Pseudo-coloring). Figure 2.1 show example of image enhancement techniques.

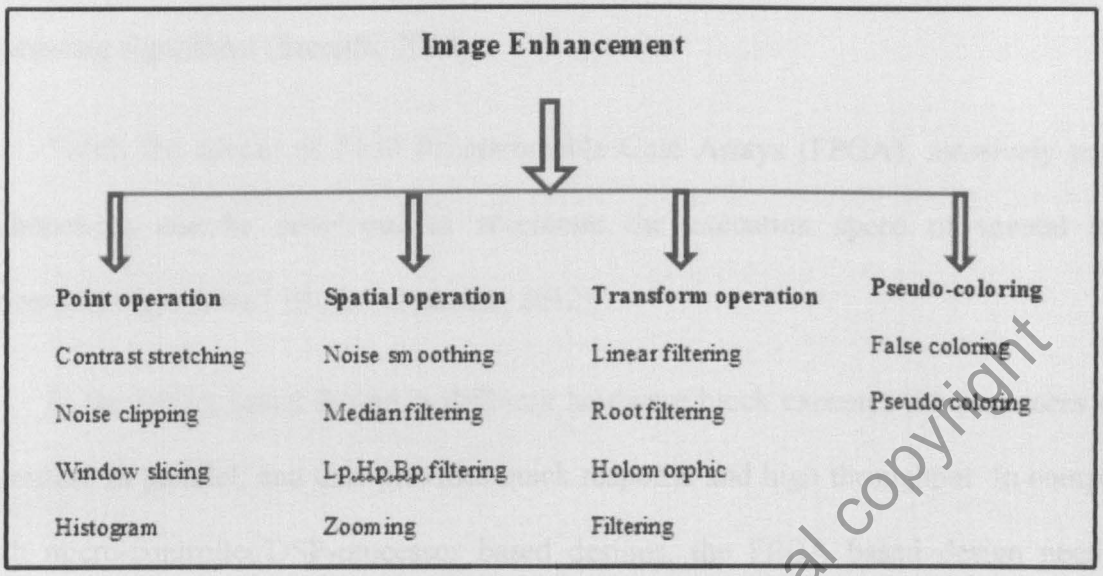

Figure 2.1: Example of Image Enhancement Techniques / Russ (2015)

Spatial domain techniques are performed to the image plane itself and they are based on direct manipulation of image pixels. The operation can be transformed as

$$f(x,y) = T[g(x,y)] \tag{2.1}$$

Where, g is the input image, T is an operation on g defined over some neighborhoods of (x,y) , and f is the output image. The operations divided into two categories: point operation and spatial operations. The spatial operations may be linear or nonlinear (Bailey, 2011).

The speed of execution is greatly increased in advanced processors that make use of pipelined and super-scalar architectures.The advanced processors incorporate parallelism at the instruction level, but the overall execution of these algorithms stay using a sequential

execution. Thus, a microcontroller is not suitable for time critical application since this system cannot effectively utilize the inherent parallelism involved in most of the image processing algorithms (Sreejith, 2014).

"With the advent of Field Programmable Gate Arrays (FPGA), massively parallel architectures can be developed to accelerate the execution speed of several image processing algorithms" (Botero-Galeano, 2012).

In the FPGA based design, a different hardware block executes the sequences of an algorithm in parallel, and thus provides quick response and high throughput. In comparing with micro-controller/DSP-processor based designs, the FPGA based design need less power consumption because of the performing of overall operations require less number of clock cycles. FPGAs are often used to implement platforms for real-time image processing applications because their structure can exploit spatial and temporal parallelism. Image processing is often considered a good candidate for parallelism.

2.2 Embedded System

An embedded system is a small computer system with a dedicated function that is embedded within a product or component. It is designed to perform one specific task, or a small range of particular tasks (Catsoulis, 2005). Often with real-time constraints, embedded system which is designed to perform image processing operations is called Embedded Imaging Systems (Bailey, 2011). The embedded image processing systems are time critical. Such systems are called as real-time systems. A real-time system is used when rigid time requirements have been placed on the operation of a processor or the flow of data; thus, it is often used as a control device in a dedicated application. In other words,

real-time systems demands response within a specified time the properties of embedded computers, when compared with general-purpose counterparts, are low power consumption, small size, rugged operating ranges. Embedded systems are cheaper than general purpose system, such as PCs since they use limited processing resources (Umbaugh, 2010). Each specific application made by an embedded system has different requirements for power supply, storage, processing, and communication. In general, the embedded system consists of four main layers: application hardware layer, application software layer, communication structure, and control structure. The layer of application hardware is responsible for interacting with the environment, while application software layer runs on the microcontroller. The task of communication part is to provide the approaches to establishing communication between different components within the system for different purposes like the need for memory or resources access. The goal of the control part is to control the priority of processes, resources administration (Henzinger & Sifakis, 2007). In the last years, there was a rapid progress in this field which resulting in reducing the component costs while increasing the microcontrollers and hardware parts.

However, the embedded system developers have to take into their consideration when designing a system that it should be low cost, high performance with minimum time to market for the competition reasons .In order to meet the requirements for a specific implementation on a platform, the key-way is to design an embedded system which has the control over the interacting between the computation and both reaction and execution constraints (Stankovic, Lee, Mok & Rajkumar, 2005). Figure 2.2 show the embedded system components.