SWITCHING TECHNIQUE OF HARMONIC ELIMINATION PULSE WIDTH MODULATION FOR FIVE-PHASE MULTILEVEL INVERTER

by

Muhammad Sirajuddin Bin Muhammad Azhar Walter
(1930913104)

A thesis submitted in fulfillment of the requirements for the degree of
Master of Science in Electrical System Engineering

Faculty of Engineering Technology
UNIVERSITI MALAYSIA PERLIS

2021

ACKNOWLEDGEMENT

Alhamdulillah, thankful to Allah for giving me the strength and courage to complete this project. My highest appreciations and gratitude towards my supervisor, Assoc. Prof. Ts. Dr. Baharuddin Ismail for his unconditional support and advice throughout the research. His guidance, encouragement, kindness, understanding and patients in handling me, ideas contributed, and support were greatly helpful. Even during the time of pandemic and with his busy schedule, he spent a considerable amount of time to help me through this project. Nevertheless, my co-supervisor, En. Muhammad Zaid Aihsan for all the support given. For all the extra explanations and guidance on the research, traveling all the way to us at Campus Pauh Putra from Campus Padang Besar for some discussions and suggestions, following and supporting us from time to time during the research period.

My appreciation also goes to my family who has been so tolerant and supports me all these years. Thanks for their encouragement, love and emotional supports that they had given to me. I would also like to thank for the lab technician for their co-operation, guidance and help in this research. Nevertheless, my great appreciation dedicated to all my friends and research team that involves directly or in directly with this research. Thanks to all supports and helps.

TABLE OF CONTENTS

PAGE

DECLARATION OF THESIS **i**

ACKNOWLEDGEMENT **ii**

TABLE OF CONTENTS **iii**

LIST OF TABLES **vi**

LIST OF FIGURES **vii**

LIST OF ABBREVIATIONS **xii**

LIST OF SYMBOLS **xiii**

ABSTRAK **xiv**

ABSTRACT **xv**

CHAPTER 1 : INTRODUCTION **1**

1.1 Research Background 1

1.2 Problem Statement 4

1.3 Research Objective 5

1.4 Research Question 6

1.5 Research Scope 6

1.6 Thesis Outline 7

CHAPTER 2 : Literature Review **9**

2.1 Introduction 9

2.2 Inverter Topologies 9

  2.2.1 Diode Clamped Inverter 11

2.2.2 Flying Capacitor Inverter 11

2.2.3 Cascaded Multilevel Inverter 12

2.3 Total Harmonic Distortion 15

2.4 Harmonic Elimination Techniques 17

2.5 Harmonic Elimination Pulse Width Modulation (HEPWM) for Cascaded Multilevel Inverter 19

2.6 Soft Computing (SC) Techniques 23

2.6.1 Genetic Algorithm 24

2.6.2 Newton-Raphson 25

2.6.3 Particle Swarm Optimization 26

2.7 Summary 30

CHAPTER 3 : Methodology 31

3.1 Introduction 31

3.2 Research Design 31

3.3 Problem Formulation 34

3.3.1 Seven-level HEPWM Using Non-notch Technique 35

3.3.2 Seven-level HEPWM Using Notch Technique 37

3.4 Optimization Solving Technique 39

3.5 Population and Samples 43

3.6 Instrumentation 44

3.7 Design of Five-Phase Seven-Level Cascaded Multilevel Inverter Simulation using PSIM 45

3.8 Insertion of Switching Angles to Field-Programmable Gate Array (FPGA) Controller 46

3.9 Hardware Validation of Five-Phase Seven-Level Cascaded Multilevel Inverter for Non-notch and Notch Switching Technique 50

3.10 Summary 51

CHAPTER 4 : Results and Discussion 52

4.1 Introduction 52

4.2 Switching Angles Computation 52

4.2.1 Switching Angles for Non-notch Seven-level Cascaded Multilevel Inverter 53

4.2.2 Switching Angles for Notch Seven-level Cascaded Multilevel Inverter 55

4.3 Simulation and Experimental Results 57

4.3.1 Seven-Level Non-Notch Waveforms 58

4.3.2 Seven-Level Notch Switching Waveforms 72

4.4 Summary 90

CHAPTER 5 : Conclusion 91

5.1 Achieved Outcome 91

5.2 Recommendation for Future Work 92

REFERENCES 93

APPENDIX A LIST OF PUBLICATION 104

LIST OF TABLES

PAGE

Table 2.1 : Difference between cascaded multilevel, flying capacitor and diode clamped 10

Table 2.2 : Summary of harmonic order for different standards 16

Table 2.3 : Summary of the HEPWM related work using multiple technique 22

Table 2.4 : Summary of PSO related work in previous research 29

Table 3.1 **:** Population and paramaters used 44

Table 4.1 : Measured simulation and experimental individual harmonics component in percentage for 0.65 and 0.85 modulation index for non-notch switching 71

Table 4.2 : Measured simulation and experimental individual harmonics component in percentage for 0.65 and 0.85 modulation index for notch switching 88

Table 4.3 : Percentage of error for THD of 0.65 and 0.85 modulation index non-notch and notch swtching technique 90

LIST OF FIGURES

PAGE

Figure 2.1 : Circuit model of seven-level five-phase cascaded multilevel inverter 15

Figure 3.1 : The flowchart of research 33

Figure 3.2 **:** General waveform for non-notch seven-level inverter 36

Figure 3.3 : General waveform for notch seven-level inverter 38

Figure 3.4 : Flowchart of the PSO algorithm 42

Figure 3.5 : Actual simulation circuit constructed using PSIM 46

Figure 3.6 : Switching angles insertion template for FPGA 47

Figure 3.7 : Switching angles insertion for non-notch 0.65 modulation index 48

Figure 3.8 : Switching angles insertion for notch 0.65 modulation index 49

Figure 3.9 : Experimental setup for validation purpose 51

Figure 4.1 : Switching angles for non-notch switchings 54

Figure 4.2 : Percentage of 3^{rd} and 7^{th} harmonic againts modulation index 54

Figure 4.3 : Switching angles for notch switching 56

Figure 4.4 : Percentage of harmonic against modulation index for 3/5/9 switching distribution 56

Figure 4.5: THD graph for simulation with 3/5/9 switching distribution 57

Figure 4.6 : Simulation results of 0.65 modulation index for five-phase seven-level cascaded multilevel inverter non-notch type (a) Phase voltage output waveform (b) Harmonic spectrum of the phase voltage output 59

Figure 4.7 : Enlargement for simulation results of 0.65 modulation index for five-phase seven-level cascaded multilevel inverter non-notch type (a) Phase voltage (V_{AN}) output waveform (b) Harmonic spectrum of the phase voltage (V_{AN}) 60

Figure 4.8 **:** Experimental results of 0.65 modulation index for five-phase seven-level cascaded multilevel inverter non-notch type phase voltage (V_{AN}) output waveform and harmonic spectrum of the phase voltage (V_{AN}) 61

Figure 4.9 : Simulation results of 0.65 modulation index for five-phase seven-level cascaded multilevel inverter non-notch type (a) Line-to-line output waveform (b) Harmonic spectrum of the line-to-line output voltage 62

Figure 4.10 : Enlargement for simulation results of 0.65 modulation index for five-phase seven-level cascaded multilevel inverter non-notch type (a) Line-to-line (V_{AB}) output waveform (b) Harmonic spectrum of the line-to-line voltage (V_{AB}) 63

Figure 4.11 : Experimental results of 0.65 modulation index for five-phase seven-level cascaded multilevel inverter non-notch type line-to-line output waveform (V_{AB}) and harmonic spectrum of the line-to-line output voltage (V_{AB}) 64

Figure 4.12 : Simulation results of 0.85 modulation index for five-phase seven-level cascaded multilevel inverter non-notch type (a) Phase voltage output waveform (b) Harmonic spectrum of the phase voltage output 65

Figure 4.13 : Enlargement for simulation results of 0.85 modulation index for five-phase seven-level cascaded multilevel inverter non-notch type (a) Phase voltage output waveform (V_{AN}) (b) Harmonic spectrum of the phase voltage (V_{AN}) 66

Figure 4.14 **:** Experimental results of 0.85 modulation index for five-phase seven-level cascaded multilevel inverter non-notch type phase voltage output waveform (V_{AN}) and harmonic spectrum of the phase voltage (V_{AN}) 67

Figure 4.15 : Simulation results of 0.85 modulation index for five-phase seven-level cascaded multilevel inverter non-notch type (a) Line-to-line output waveform (b) Harmonic spectrum of the line-to-line output voltage 68

Figure 4.16 : Enlargement for simulation results of 0.85 modulation index for five-phase seven-level cascaded multilevel inverter non-notch type (a) Line-to-line (V_{AB}) output waveform (b) Harmonic spectrum of the line-to-line voltage (V_{AB}) 69

Figure 4.17 : Experimental results of 0.85 modulation index for five-phase seven-level cascaded multilevel inverter non-notch type line-to-line output waveform (V_{AB}) and harmonic spectrum of the line-to-line output voltage 70

Figure 4.18 : Half-wave cycle waveform of 3/5/9 switching distribution for (a) 0.65 modulation index (b) 0.85 modulation index 74

Figure 4.19 : Simulation results of 0.65 modulation index for five-phase seven-level cascaded multilevel inverter notch type (a) Phase voltage output waveform (b) Harmonic spectrum of the phase voltage output 76

Figure 4.20 : Enlargement for simulation results of 0.65 modulation index for five-phase seven-level cascaded multilevel inverter notch

type (a) Phase voltage output waveform (V_{AN}) (b) Harmonic spectrum of the phase voltage (V_{AN}) 77

Figure 4.21 : Experimental results of 0.65 modulation index for five-phase seven-level cascaded multilevel inverter notch type phase voltage output waveform (V_{AN}) and harmonic spectrum of the phase voltage (V_{AN}) 78

Figure 4.22 : Simulation results of 0.65 modulation index for five-phase seven-level cascaded multilevel inverter notch type (a) Line-to-line output waveform (b) Harmonic spectrum of the line-to-line output voltage 79

Figure 4.23 : Enlargement for simulation results of 0.65 modulation index for five-phase seven-level cascaded multilevel inverter notch type (a) Line-to-line (V_{AB}) output waveform (b) Harmonic spectrum of the line-to-line voltage (V_{AB}) 80

Figure 4.24 : Experimental results of 0.65 modulation index for five-phase seven-level cascaded multilevel inverter notch type line-to-line output waveform (V_{AB}) and harmonic spectrum of the line-to-line voltage 81

Figure 4.25 : Simulation results of 0.85 modulation index for five-phase seven-level cascaded multilevel inverter notch type (a) Phase voltage output waveform (b) Harmonic spectrum of the phase voltage output 82

Figure 4.26 : Enlargement for simulation results of 0.85 modulation index for five-phase seven-level cascaded multilevel inverter notch type (a) Phase voltage output waveform (V_{AN}) (b) Harmonic spectrum of the phase voltage (V_{AN}) 83

Figure 4.27 : Experimental results of 0.85 modulation index for five-phase seven-level cascaded multilevel inverter notch type phase

voltage output waveform (V_{AN}) and harmonic spectrum of the phase voltage 84

Figure 4.28 : Simulation results of 0.85 modulation index for five-phase seven-level cascaded multilevel inverter notch type (a) Line-to-line output waveform (b) Harmonic spectrum of the line-to-line output voltage 85

Figure 4.29 : Enlargement for simulation results of 0.85 modulation index for five-phase seven-level cascaded multilevel inverter notch type (a) Line-to-line (V_{AB}) output waveform (b) Harmonic spectrum of the line-to-line voltage (V_{AB}) 86

Figure 4.30 : Experimental results of 0.85 modulation index for five-phase seven-level cascaded multilevel inverter notch type line-to-line output waveform (V_{AB}) and harmonic spectrum of the line-to-line voltage 87

LIST OF ABBREVIATIONS

AC	Alternating Current
APOD	Alternating Phase Opposite Disposition
CHMI	Cascaded H-bridge Multilevel Inverter
CMV	Common-mode voltage
CSI	Current Source Inverter
DC	Direct Current
FPGA	Field-Programmable Gate Array
GA	Genetic Algorithm
HEPWM	Harmonic Elimination Pulse Width Modulation
Hz	Hertz
MGA	Modified Genetic Algorithm
MVSI	Multilevel Voltage Source Inverter
NR	Newton-Raphson
OMTHD	Optimal Minimization Total Harmonic Distortion
PD	Phase Disposition
POD	Phase Opposite Disposition
PSIM	Software for Power Electronics Simulation
PSO	Particle Swarm Optimization
PWM	Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
VSI	Voltage Source Inverter

LIST OF SYMBOLS

θ	Switching Angle
C_1, C_2	Constriction factors
G_{best}	Global best
k	Harmonics order
M	Modulation Index
P_{best}	Present best
S	Number of eliminated harmonic
V_1	Fundamental voltage component
V_{AN}	Phase A voltage respect to neutral point
V_{BN}	Phase B voltage respect to neutral point
V_{CN}	Phase C voltage respect to neutral point
V_{DN}	Phase D voltage respect to neutral point
V_{EN}	Phase E voltage respect to neutral point
V_{AB}	Line-to-line voltage between phase A and B
V_{BC}	Line-to-line voltage between phase B and C
V_{CD}	Line-to-line voltage between phase C and D
V_{DE}	Line-to-line voltage between phase D and E
V_{EA}	Line-to-line voltage between phase E and A
V_{dc}	Input DC voltage
W	Inertia Weight

Teknik Pensuisan bagi Penghapusan Harmonik Modulasi Lebar Denyut untuk Penyongsang Lima-Fasa Berbilang Aras

ABSTRAK

Kajian ini bertumpukan kepada teknik pensuisan bagi penghapusan harmonik modulasi lebar denyut untuk penyongsang lima-fasa berbilang aras. Penyongsang berbilang aras adalah salah satu mekanisme pensuisan yang sering digunapakai. Walaubagaimanapun, pensuisan ini boleh menyebabkan harmonik dimana ia sering berlaku didalam sistem kuasa kerana herotan dan boleh menyebabkan banyak masalah yang tidak diingini. Ia boleh berlaku samaada pada bentuk gelombang voltan atau arus elektrik. Pengurangan minimum terhadap herotan jumlah harmonik (THD) sangat perlu dalam menjaga sistem kuasa yang bagus. Teknik pensuisan yang disarankan untuk penyongsang lataan lima-fasa berbilang aras yang digunakan dalam penyelidikan ini ialah teknik pensuisan *non-notch* dan *notch*. Algorithma PSO telah digunakan sebagai teknik pengoptimuman dalam mencari sudut-sudut pensuisan untuk teknik pensuisan *non-notch* dan *notch*. Tambahan pula, simulasi penyongsang lataan tujuh-aras lima-fasa untuk kedua-dua operasi pensuisan telah dijalankan menggunakan PSIM. Hasil diperolehi menunjukkan bahawa pensuisan *non-notch* mampu menghapus harmonik aturan rendah sehingga harmonik ke-7. Seterusnya, teknik pensuisan *notch* pula mampu menghapuskan harmonik aturan rendah sehingga harmonik ke-41 dengan pengedaran pensuisan 3/5/9. Ini mengesahkan bahawasa sudut pensuisan yang diperolehi daripada PSO itu telah dinilai. Kelebihan teknik pensuisan *notch* telah disahkan oleh hasil simulasi, dimana harmonik ke-3,7,9,11,13,17,19,21,23,27,29,31,33,37,39, dan 41 telah berjaya dihapuskan. Hasil yang diperolehi bagi keseluruhan index modulasi ialah daripada 0.50 sehingga ke 0.90 untuk pengsuisan *non-notch*. Manakala bagi pensuisan *notch*, index modulasi 0.60 sehingga 0.90 yang mempunyai penyelesaian. Untuk penyelidikan ini, hanya index modulasi 0.65 dan 0.85 dipilih bagi tujuan pengkajian. Keberkesanan teknik pensuisan *notch* dalam pengurangan THD untuk sesebuah sistem telah pun terbukti. Keputusan-keputusan simulasi yang diperolehi jugak telah disahkan dengan konfigurasi perkakasan. Keputusan menunjukkan bahawa THD bagi index modulasi 0.65 adalah 5.34% dan bagi index modulasi 0.85 adalah 1.72%. Adalah dijangkakan bahawa HEPWM yang dicadangkan adalah sangat berguna untuk reka bentuk penyongsang lataan tujuh-aras lima-fasa yang secara praktikalnya mempunyai prestasi yang lebih tinggi dan kos yang rendah.

Switching Technique of Harmonic Elimination Pulse Width Modulation for Five-Phase Multilevel Inverter

ABSTRACT

This research focuses on the switching technique of harmonic elimination pulse width modulation for five-phase multilevel inverter. Multilevel inverters are one of the most commonly used switching mechanisms. However, this switching may cause harmonics which usually occur in a power system due to distortion and can cause a lot of unwanted problems. It could appear in either voltage or current waveforms. Minimization of Total Harmonic Distortion (THD) is necessary in order to maintain a good power system. The proposed switching technique for five-phase cascaded multilevel inverter used in this research is non-notch and notch switching technique. Particle Swarm Optimization (PSO) algorithm was used as an optimization technique to find switching angles for non-notch and notch switching techniques. In addition, the simulation of a seven-level five-phase cascaded multilevel inverter for both switching operations is carried out in the PSIM environment. The results show that the non-notch switching was able to eliminate lower order harmonics up to the 7th harmonic. Next, the notch switching technique managed to eliminate lower order harmonics up to the 41st harmonic with 3/5/9 switching distribution. This verified that switching angles obtained from the PSO were evaluated. The advantage of this notch switching technique was confirmed by the simulation results, where the 3rd, 7th, 9th, 11th, 13th, 17th, 19th, 21st, 23rd, 27th, 29th, 31st, 33rd, 37th, 39th, and 41st harmonics are successfully eliminated. The results were obtained for an entire modulation index of 0.50 to 0.90 for non-notch switching. While for notch switching, modulation index of 0.60 to 0.90 were provided with solutions. For this research, modulation index of 0.65 and 0.85 was chosen to be experimented. The effectiveness of a notch switching scheme in reducing THD for a system was proven. Obtain simulations results were also verified with hardware configuration. The results show that the THD for modulation index 0.65 is 5.34% and for modulation index 0.85 is 1.72%. It is envisaged that the proposed HEPWM can be very useful in the design of a practical high performance and low cost five-phase cascaded multilevel inverter.

CHAPTER 1 : INTRODUCTION

1.1 Research Background

In recent years, multilevel voltage source inverter (MVSI) has attracted many researchers' attention. This is because the multilevel inverter can produce a high output voltage even when it only uses power switches with a lower rating (Zhu et al., 2020). An inverter is also known as a converter that converts DC to AC power (Shen et al., 2014; Khan et al., 2020). It also uses a standard low voltage component configuration; thus, it can save cost. Moreover, the higher the level of the inverter, the lower the harmonic becomes (Taghizadeh & Tarafdar Hagh, 2010; Ahmed et al., 2018). However, increasing the level of inverter then leads to more costing and space consuming.

Many types of MVSI topologies have been developed over the past few years. The three main topologies are known as cascaded H-Bridge (CHB), Flying Capacitor and Diode Clamped (Mhiesan et al., 2019). CHB is one of the famous topologies used among researchers due to its advantages compared to flying capacitor and diode clamped (Malinowski et al., 2010; Maheswari et al., 2021). Koshti et al., (2017) work build topology that can produce high voltage capabilities and high-power quality. Increasing the inverter level reduces the THD in the system. This will improve the quality of the power supply (Hagh et al., 2017).

One of the main differences between single-phase and three-phase is the amount of power given (Bellar et al., 2004; Anderson et al., 2021). This is because three-phase power supply can transmit three times as much power as a single-phase power supply.

Aside from that, three-phase also have better consistency in delivering the power rather than single-phase. This is also applied for five-phase system. This is because of the peaks and dips in voltage. Ranjram et al, (2020) work shows that five-phase power supply can deliver power at a steady and constant rate when compared to a single-phase. Three-phase or five-phase power supplies are also more efficient. A three-phase power supply can provide three times the power of a single-phase power supply, and a five-phase power supply can provide five times the power of a single-phase power supply (Yang & Tolle, 2019).

A five-phase system is also well suited for high fault tolerance and high efficiency (Priestley et al., 2018). Other than that, multiphase systems such as five-phase are getting attention due to their advantages, such as reduced amplitude and increased frequency of torque pulsation, reduced dc-link current harmonics, reduced size due to higher power density, and reduced current per phase compared with traditional three-phase drives (Sakthisudhursun et al., 2016; Karampuri et al., 2019).

An inverter involves switching in the system. There are a variety of switching schemes that can be applied to the system. One of the famous switching methods used is called Harmonic Elimination Pulse Width Modulation (HEPWM) (Dahidah et al., 2015). This method can be used to eliminate specific harmonics, reduce THD, and achieve a smoother transition between phases (Srndovic et al., 2018; K, Sharifzadeh M, Vahedi H, 2019). However, determining the optimum HEPWM switching angle will be extremely difficult. This is due to its non-linear transcendental equation (M. S. Patil et al., 2016). This calculation was complex and required the use of an algorithm to solve.

One of the most effective algorithms for solving these equations is known as the Particle Swarm Optimization algorithm. PSO was first introduced by Kennedy and Eberhart in 1995 based on the behavior of a social system such as fish schooling and birds flocking (James Kennedy; Russell Eberhart, 1995). It has much faster convergence with better quality solutions compared to other algorithms.

This algorithm was tested using a seven-level five-phase cascaded multilevel inverter. Since seven-level cascaded multilevel inverter was commonly used in many previous researches, it was implemented here. By finding the optimum switching angle for this system, it will specifically suppress any order of harmonics in the system. The switching angle for both single switching (non-notch types) and multiple switching (notch types) has been calculated. The algorithm was developed in the MATLAB environment. The angle obtained was then tested by PSIM simulation and validated using hardware configurations.

In this research, the effectiveness of an optimization algorithm to solve the HEPWM switching angles problems was validated using a seven-level five-phase inverter. It was also tested for both switching scheme, non-notch and notch type. The obtained switching angles were then simulated with PSIM and experimentally validated. When compared to the conventional method, this method allows for the elimination of more harmonics while not increasing the levels of cascaded multilevel inverter.

1.2 Problem Statement

Industries are consistently in demand for better efficiency and higher motor output power from AC drives system. A three-phase system is more popular than a five-phase system because it is less expensive and more economical. Considering its shortcoming to a five-phase system, the three-phase system is subjected to extra vibration for the motor because of larger stepping angle (120º) for each phase compared to a five-phase system that has smaller phase angle between phases (72º) to provide smoother operation. In the event of one of the phase failures or damaged, the three-phase system will stop operating, whereas the five-phase system is expected to continue operation even though one or two of the phases loss connection. Additionally, the five-phase system can also withstand much higher power to produce higher torque demand to the motor.

Other than that, harmonic distortion is a significant issue in an electrical phase system. Typically, these unwanted distortions will increase the output power, which results in higher temperatures and audible noise emissions when compared to sinusoidal excitation. This will decrease the lifespan of the motor, affects the efficiency of the output and increase losses throughout the system. Lower order harmonics always contribute the most harmonic distortion. To eliminate these harmonics, HEPWM switching pulses for the five-phase cascaded multilevel inverter are proposed as a solution. The benefit of this method is that it is capable of solving a non-linear equation associated with HEPWM for the five-phase cascaded multilevel inverter. In addition, with the precision switching angles, the unwanted harmonics can be eliminated, and the output voltage produced is expected to be of high quality voltage. Furthermore, by using this method, the elimination of selected harmonics could minimize the Total Harmonic Distortion (THD) and losses.

HEPWM is normally used by researchers for single switching known as the non-notch switching technique. This limits the number of harmonics that can be eliminated, as it depends on the level of the inverter. Thus, using the non-notch technique by just increasing the level of the inverter to eliminate more harmonics could lead to increased complexity of the circuit and increase the cost for building it. Therefore, in order to eliminate more harmonics, notch switching technique was proposed. This will increase the amount of switching angles and, as a result, increases the number of harmonics that can be eliminated from the system. Optimum switching angles can be generated using an optimization in order to control the harmonics of the system. This could help in eliminating a higher number of harmonics at once, suppressing the THD in the system.

1.3 Research Objective

The objectives of the project are:

1. To design the HEPWM switching technique and calculate the switching angles by using Particle Swarm Optimization.

2. To design a seven-level cascaded multilevel inverter for five-phase system.

3. To evaluate the effectiveness of five-phase multilevel inverter with non-notch and notch switching for various modulation index.

1.4 Research Question

1. How to develop a high output voltage source with low THD for a five-phase system?

2. How to solve the switching angles needed without consuming a lot of time?

3. What method of switching can be implemented to improve the system performance for THD?

1.5 Research Scope

The scope of this research will mainly be focused on designing five-phase system for seven-level cascaded inverter with equal DC sources. With optimization algorithm, and use of PSIM, simulations will be used for study purpose. All the results will be collected for analyzing the proposed system. In precisely, project scope as follows:

1. To design the HEPWM non-notch and notch for seven-level cascaded multilevel inverter.

2. A topology of a five-phase seven-level cascaded multilevel inverter with equal DC sources and PSO algorithm are applied for this system.

3. Switching angles obtained from PSO are simulated with five-phase seven-level cascaded multilevel inverter for 50 Hz which was the fundamental frequency using PSIM software.

4. By varying parameters, find the optimum solutions for a wider range of modulation index. Then select the best optimum solutions of switching angles to perform for hardware validations.

5. Evaluate individual harmonic eliminations for standard verifications given by IEC EN50160 (2004), CIGRE JWG C4.07 (2004), IEC 6100-3-6 (1996) and tabulate the data precisely.

1.6 Thesis Outline

This report consists of five chapters, which are divided into Chapter 1, Chapter 2, Chapter 3, Chapter 4 and Chapter 5.

Chapter 1 discuss the overview of the project background. The problem statement, the objectives, and project scope are also discussed in this chapter.

Chapter 2 discuss the literature review thoroughly. The discussion includes the topology of multilevel inverter, switching technique and algorithm use to find switching angles. This chapter also reviews the related work from the previous project.

Chapter 3 is the methodology, which describes project flowchart, project design and the development of the project. This chapter also explains about the software design and algorithm technique.

Chapter 4 presents the results and discussion that are obtained from the simulations application and hardware configurations.

Chapter 5 discuss about the overall conclusion of the developed projects, recommendation and future developments.

CHAPTER 2 : LITERATURE REVIEW

2.1 Introduction

In this chapter, topology of cascaded multilevel inverter and its operation are reviewed. The topologies of inverter are discussed at the beginning of the chapter. Cascaded multilevel circuitry are also shown. Then, followed by allowable limit of Total Harmonic Distortion (THD) for the system. Switching scheme of Harmonic Elimination Pulse Width Modulation are discussed with the difference between single switching scheme (non-notch) and multiple switching scheme (notch). Next, algorithm used in solving the calculation to obtain the optimum switching angles are also explained. Among these discussions, previous works are also critically reviewed in this chapter. Finally, the summary of the chapter is presented at the end of the chapter.

2.2 Inverter Topologies

Inverter is also known as converter which convert DC-AC power output. An inverter is most commonly used switching mechanism. There are many types of inverter such as Current Source Inverter (CSI) and Voltage Source Inverter (VSI). VSI is known as two-level or multilevel voltage source inverter (MVSI). H-bridge of MVSI is called Cascaded H-Bridge Multilevel Inverter. This is the focus of this research work.

The three main topologies well known in inverter are flying capacitor, diode clamped, and cascaded H-bridge (Krishna & Suresh, 2016; Hota et al., 2017). The era of multilevel inverter started with diode clamped around 1981, followed by flying