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Reliability Comparison between Solder and Solderless Flip Chip Interconnection In Terms of High Temperature Storage

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Abstract. Flip chip (FC) has been used to replace wire bond due to its better performance. The 1st interconnection in FC plays an important role in terms of reliability study. Au/Cu stud bump capped with Sn tends to have Kirkendall void in the joint which can cause open circuit. This paper focuses on depth analysis on solderless chip bumping by using only Cu stud bump in the chip on chip (CoC) ball grid array (BGA) package. High temperature storage 150 °C has been applied on package and the result was compared with those the use of Au stud bump capped with Sn. The result shows that Cu stud bump has a better reliability in term of electrical resistance compared with Au stud bump capped with Sn. Therefore, solderless chip bumping has the potential to replace Au stud bump capped with Sn for FC BGA package.

Keywords: Flip chip, Cu stud bump, Kirkendall void, CoC

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INTRODUCTION

FC is another interconnection method that provides the same function as wire bond which involves the chip with bumps face down and is connected to the substrate via bumps. FC technology has been growing rapidly in the semiconductor technology which is opting for smaller dimension while preserving and improving the performance of the multi-function electronic devices. Moreover, FC technology shows better reliability in terms of thermal and electrical performances. In addition to this, it also has a higher packaging density and involves a lower cost as compared to conventional method such as wire bond [1]. FC attachment and chip bumping are the FC assembly in 1st interconnection. Thermocopression and thermosonic are the common practice for the attachment while lead free solder, Cu pillar or Au stud bump are the chip bumpings.

However, the usage of Au/Cu stud bump capped with Sn in chip bumping results in Kirkendall void. The Kirkendall void is caused by the growth of the thickness of intermetallic compound between Cu/Au and Sn which may affect the reliability of the package [2]. AuSn is formed at the joint and the Intermetallic Compound (IMC) is brittle. Therefore, solderless chip bumping is another alternative for chip bumping [3-8].

Thermosonic flip chip bonding (TSB FC) has advantages over the thermocompression flip chip bonding (TCB FC). TSB FC has been demonstrated in this work and the reliability of solderless chip bumping is compared with Au stud bump capped with lead free solder in this report.

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EXPERIMENTAL PROCEDURE

The development of the Cu stud bump and the thermosonic bonding (TSB) FC has been reported before [9-10]. Therefore the experiment is focused on the reliability stress test. Figure 1 shows the process flow of the reliability stress test. The samples undergo high temperature storage at 150 °C up to 1008 hour (h). The electrical resistance was measured at each read point. This experiment electrical resistance was compared with Orii works who used Au stud bump capped with Sn by using thermocompression bonding (TCB) [11]. The failure criteria is 20% electrical resistance increment from the initial value [12-14].

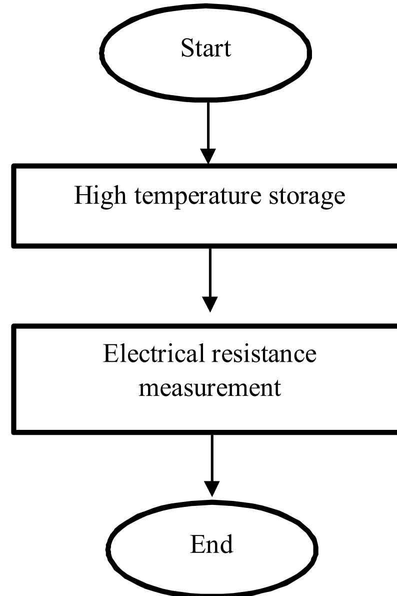

FIGURE 1. Process flow for high temperature storage reliability stress test

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RESULTS AND DISCUSSION

All samples passed the electrical testing after being subjected to HTS 168 h, 504 h, and 1008 h according to industry standard. Table 1 summarizes the electrical testing results at every read point after being subjected to HTS 150 °C. The failure criterion is an increment of 20% of initial electrical resistance [12-14].

TABLE 1. O/S test after HTS

HTS 150 °C	Test result
168h	Pass
504h	Pass
1008h	Pass

Figure 2 shows the electrical resistance versus HTS between this work and other researchers'. The electrical resistance slowly increased and did not exceed 20% of initial value after 1008 h in this work. One of the closest researches to this work was done by Orii. From the literature review, there was no research done as yet on the reliability

stress test in TSB. In view of this, in order to compare with other researchers' work, the TCB stress test results using the same method as this work as reported by Orii were taken as comparison. The electrical resistance increased drastically and reach 20% of increment during 250 h of HTS in Orii's work.

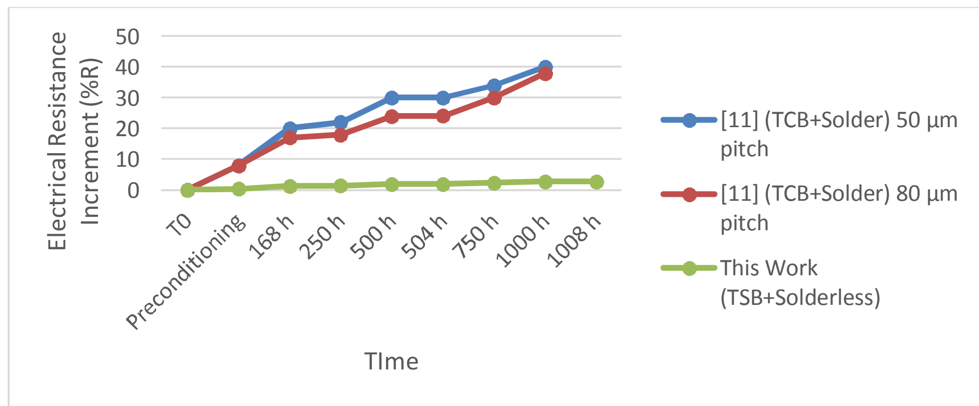

FIGURE 2. Electrical resistance increment versus HTS

Refering to Orii result, the SEM image from Orii's work shows the Au and Al interface. Many Kirkendall voids were found at the boundary of Au and Al of Orii's work after HTS test. In their work, Au stud bump shape has also been changed after HTS test and it appeared to be diffused away. The small voids accumulated land created a crack [11]. Orii's work has discovered that many Kirkendall voids were found at the boundary at Au/Al after reliability stress test. In their work, the Au stud bump shape has also been changed. In contrast, there was no Kirkendall issue in this work after HTS 1008 h was applied on TSB sample.

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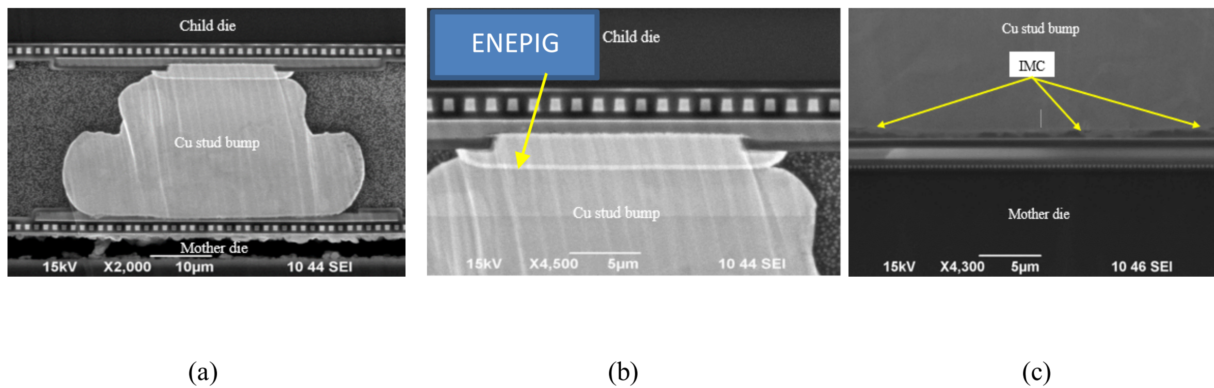

(a) (b) (c)

FIGURE 3. HTS condition at 150 °C for 1008 h (a) overall (b) top joint & (c) bottom joint

Figure 3 shows cross section images of the bond interface after the samples were subjected to HTS 150 °C for 1008 h. Significant IMC growth was clearly observed when the aging time was continuously increased. The Al layer has still not yet been fully consumed. There was no significant IMC observed between Cu and ENEPIG interface throughout HTS test. The IMC at the bottom joint (Cu/Al) grew along with the aging time. However, the top joint (Cu/ENEPIG) did not show any obvious IMC thickness. In Ratchev research, there was also no obvious IMC found between Cu and ENEPIG after thermal aging 150 °C [15].

CONCLUSION

In HTS, the TSB sample passed the O/S test even after HTS 1008 h. The electrical resistance of this work is much lower compared with other research works and not exceeded 20% increment from the initial electrical resistance value. Hence, this clearly proved that the solderless Cu stud bump joint tends to have a better performance as compared to those where Au stud bump and lead free solder are applied.

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REFERENCE

1. Palesko, C. A., & Vardaman, E. J. (2010). Cost comparison for flip chip, gold wire bond, and copper wire bond packaging. In *2010 Proceedings 60th Electronic Components and Technology Conference (ECTC)* (pp. 10–13).
2. Park, J.-M., Kim, S.-H., Jeong, M.-H., and Park, Y.-B. (2014). Effect of Cu–Sn intermetallic compound reactions on the Kirkendall void growth characteristics in Cu/Sn/Cu microbumps. *Japanese Journal of Applied Physics*, *53*(5S3), 05HA06.
3. Pan, J., Silk, J., Powers, M., & Hyland, P. (2011). Effect of Gold Content on the Reliability of SnAgCu Solder Joints. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, *1*(10), 1662–1669.
4. Lee, Y.-K., Ko, Y.-H., Kim, J.-K., Lee, C.-W., & Yoo, S. (2013). The effect of intermetallic compound evolution on the fracture behavior of Au stud bumps joined with Sn-3.5Ag solder. *Electronic Materials Letters*, *9*(1), 31–39.
5. Guth, K., Oeschler, N., Boewer, L., Speckels, R., Strotmann, G., Heuck, N., et al. (2012). New assembly and interconnect technologies for power modules. In *2012 7th International Conference on Integrated Power Electronics Systems (CIPS)* (pp. 1–5).
6. Wen, F. B., Krishnan, S., & Chan, Y. M. (2008). Lead-free solder paste selection and solder joint reliability for copper stud flip chip. In *2008 International Conference on Electronic Materials and Packaging* (pp. 80–83).
7. Lee, J. H., Song, J. Y., Ha, T. H., Lee, C. W., Kim, S. M., Kim, Y. J., & Lee, Y. K. (2015). Investigation of fracture mechanisms and bond-line of insert bump bonding specimens. In *2015 European Microelectronics Packaging Conference (EMPC)* (pp. 1–4).
8. Shin, J., Choi, Y., Kim, Y. S., Kang, U. B., Seo, S. K., & Paik, K. (2014). A novel double layer NCF for highly reliable micro-bump interconnection. In *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)* (pp. 1755–1758).
9. Lim, M. R., Sauli, Z., Aris, H., Retnasamy, V., Lo, C., Muniandy, K., et al., (2018). First level interconnection based on optimization of Cu stud bump for chip to chip package. *AIP Conference Proceedings*, *2045*(1), 20095.
10. Lim, M. R., Sauli, Z., Aris, H., Retnasamy, V., Lo, C., Muniandy, K., et al., (2018). The optimization of ultrasonic power and bonding time for thermosonic flip chip bonding. *AIP Conference Proceedings*, *2045*(1), 20094.
11. Orii, Y., Toriyama, K., Kohara, S., Noma, H., Okamoto, K., Toyoshima, D., et al. (2011). Micro Structure Observation and Reliability Behavior of Peripheral Flip Chip Interconnections with Solder-Capped Cu Pillar Bumps. *Transactions of The Japan Institute of Electronics Packaging*, *4*(1), 73–86.
12. Lee, C.-C., Yang, T.-F., Wu, C.-S., Kao, K.-S., Cheng, R.-C., & Chen, T.-H. (2013). Reliability estimation and failure mode prediction for 3D chip stacking package with the application of wafer-level underfill. *Microelectronic Engineering*, *107*, 107–113.
13. Wu, F., Ho, L., Kuo, C., Tu, C., Hsieh, C., Ni, C.,et al. (2013). Three dimensional interconnect using Au and pillar bumps. In *2013 IEEE 63rd Electronic Components and Technology Conference* (pp. 1933–1939).
14. Qi, H., Vichare, N. M., Azarian, M. H., & Pecht, M. (2008). Analysis of Solder Joint Failure Criteria and Measurement Techniques in the Qualification of Electronic Products. *IEEE Transactions on Components and Packaging Technologies*, *31*(2), 469–477.
15. Ratchev, P., Stoukatch, S., & Swinnen, B. (2006). Mechanical reliability of Au and Cu wire bonds to Al, Ni/Au, and Ni/Pd/Au capped Cu bond pads. *Microelectronic Reliability, 46(8)*, 1315-1325.

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