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DESIGN OF HIGH SPEED LOW POWER CMOS COMPARATOR USING FORWARD BODY BIAS TECHNIQUE

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1. Introduction

In the modern digital world, the Analog-To-Digital Converters (ADCs) play a major role in every hardware device. The speed and power consumption are the two main factors for today portable applications [1]. For past several years, the CMOS technology scaling is the most important procedure for the improvement of circuit performances such as speed, delay and power. Besides, one of the ways to minimize power consumption is by supplying voltage reduction technique as power relation to the square of supplying voltage. However, one cannot simply reduce the supply voltage as it will causes the delay problem becoming critical. Comparators are the most important circuit to control the performance and the accuracy of ADCs. There are various types of comparator architecture have been proposed for high speed [2-7]. The most popular architecture is CMOS dynamic comparators [7]. The dynamic comparators are often called as a clocked comparator due to the clock sensitive and output is responding only to the trigger of clock. In [8], a regenerative stage and interface stage of dynamic comparator are proposed.

The interface stage includes all the transistors without cross coupled inverters with two cross coupled inverters of regenerative stage. These two cross coupled inverters are invented to supply the latching in order to force a fast decision making from the input

terminal. The major drawback of the dynamic latch comparator is the unwanted power consumption caused by the circuit when the clock is low since both the outputs are pre-charged to VDD. A low power and high speed dynamic latch comparator in 0.18 μm CMOS process by using charge sharing technique is proposed in [9]. The latch circuit with high input impedance is employed in dynamic charge sharing topology. Besides, the static power dissipation is avoided by using a rail to rail output swing. Furthermore, this topology has the advantage of high immune to the parasitic capacitances of the input transistors to the output nodes [10].

However, the main problem of this circuit topology is large power consumption during reset mode in the resistive dividing circuit which causes undesired power dissipation due to charge sharing and charge leakage from the circuit. Further in [11], the conventional double-tail comparator is proposed. The main advantage of this comparator is that it can work at low voltages compared to the conventional dynamic comparator due to the less stacking of this topology. The operation of the double tail comparator is divided into two phases which are reset and comparison (decision making) phases. However, the delay is still higher eventhough the speed is high. In this paper, a comprehensive study about the speed and power of double-tail comparator has been presented. Two types of double-tail comparator of high speed and low power high speed based on architecture in [11] are proposed and simulated using 0.13-μm CMOS technology. Furthermore, high speed low power double-tail comparator using forward body bias technique is proposed to improve delay and speed with low power.

This paper is organized as follows: in Section 2, the design implementation of three architectures of double-tail comparator is discussed. Section 3 presents the design specifications of input and transistors' dimension. The simulation results achieved from the proposed comparators are presented in Section 4. Finally, Section 5 concludes overall achievement.