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Feasibility study of seven-level two-stage cascaded switch-diode multilevel inverter under different inductive loads

Abstract

Two-stage cascaded switch-diode multilevel inverter (TSCSDMI) is a modified cascaded H-bridge multilevel inverter (CHMI) with a reduced number of active power semiconductor switches. The TSCSDMI topology is constructed with two main circuit stages. The 1st stage consists of several cascaded switch-diode basic cell modules and a bypassing active power semiconductor switch, whilst the 2nd stage consists of a H-bridge module. The implementation and performance of a five-level TSCSDMI have been reported in the literature. However, the feasibility of the TSCSDMI with a higher number of voltage levels under different inductive loads has not been fully explored. Hence, this paper evaluates and analyzes the performance of seven-level TSCSDMI operating under different inductive. The analysis is conducted using PSIM simulation and the simulation results suggest that the seven-level TSCSDMI is not suitable for heavier inductive loads. For example, the output voltage waveform of seven-level TSCSDMI starts to deteriorate with an undesired voltage spike when the displacement power factor of an inductive load is equal to 0.90 or lower. The undesired voltage spike tends to worsen the total harmonic distortion (THD) of the output voltage waveform. Hence, for minimal THD operations, a seven-level TSCSDMI should be employed for applications with light inductive load.

Keywords:

Total harmonic distortion, Inverters, Semiconductor switch, Switching diodes