



**DESIGN AND CHARACTERIZATION OF  
SELF-SWITCHING DIODE AND PLANAR  
BARRIER DIODE AS HIGH-FREQUENCY  
RECTIFIERS**

by

**ZARIMAWATY BINTI ZAILAN  
(1340111057)**

A thesis submitted in fulfillment of the requirements for the degree of  
Doctor of Philosophy

**School of Microelectronic Engineering  
UNIVERSITI MALAYSIA PERLIS**

2018

## ACKNOWLEDGMENT

Praise be to Allah, His majesty for His uncountable blessings and peace be upon the Prophet Muhammad, His pure descendant and His family and His noble companions. Alhamdulillah, finally I have completed my Ph.D thesis in Microelectronic Engineering in the year of 2018. The journey towards the completion of this thesis was full of unexpected challenges and almost impossible to complete single-handedly without the help and support from others. I would like to give my heartfelt thanks to everyone who has provided me with such support.

Special thanks must go to my supervisor Dr. Shahrir Rizal Kasjoo, who is responsible for bringing me into this journey and giving me the opportunity to work in his group. Thank you very much for his encouragement, supervision and guidance throughout this whole research. His invaluable knowledge sharing had developed and extended my experiences and skills in the field of microelectronic. My appreciation also goes to my co supervisors Dr. Muammar Isa for his invaluable knowledge, help, support and encouragement especially in thesis writing. The trust and freedom given to me had made me work harder to not disappoint all of them.

Next, I would like to thank School of Microelectronic Engineering Postgraduate students for their endless support, discussion, amusement and friendship. I cannot name them all here, but I will acknowledge the part they played in my growth as a postgraduate student and more importantly, as a human being. Working with them has been fun and extremely rewarding. I wish to express my gratitude for the benefits that I have gained in sharing ideas and collaborations with the member in this group.

A special thanks to all staff members the School of Microelectronic Engineering, Universiti Malaysia Perlis (UniMAP) i.e Pn. Nor Farhani Zakaria, Dr. Nur Syakimah Ismail, Dr. Noraini Othman and Dr. Norhawati Ahmad for their valuable advices, technical discussions and contributions either directly or indirectly towards the realization of this research.

I am also very grateful to the Ministry of Higher Education, Malaysia and UniMAP for the financial support of my Ph.D study throughout this three-year's period. A big thank you also goes to the wonderful people in UniMAP for their kind support i.e Vice Chancellor, Dato' Prof. Zul Azhar Zahid Jamal. I would also like to thank Pn. Zehan Mat Saad and Pn. Nur Isyalliena Ishak for their support in managing the postgraduate and scholarship program.

My journey in the academic world would be impossible without the support from my family. There are no words to express my gratitude and thankfulness especially to my mother Azizah Yahya and my dearest husband, Dr. Mohammad Nuzaihan for their love, understanding, constant encouragement, endless supports and patience, and always pray for my success, especially when I faced difficulties. Not to forget, a very special thanks to my little prince, Aisy Darwisy Mohammad Nuzaihan. Last but not

least, I would also like to thank my siblings and family-in-law for their devoted love, confidence and support throughout my study, thus always encouraged me and elevated my spirit. To my friends whose names are not included here, may ALLAH bless all of us, Amin.

Thanks to Almighty ALLAH.

©This item is protected by original copyright

*Al-Fatihah special dedication to my late grandparents and parents in laws. May Allah S.W.T bless them, Amin.*

*To my mom, thank you for everything that you've poured into my life.*

*To my lovely husband, Mohammad Nuzaihan, for devoted love and support.*

*To my son, Aisy Darwisy for cheerfulness.*

*To my brother, thank you for your supportive.*

*To my family-in-law for being a part of my life.*

©This item is protected by original copyright

## TABLE OF CONTENTS

	<b>PAGE</b>
<b>DECLARATION OF THESIS</b>	<b>i</b>
<b>ACKNOWLEDGMENT</b>	<b>ii</b>
<b>TABLE OF CONTENTS</b>	<b>v</b>
<b>LIST OF TABLES</b>	<b>ix</b>
<b>LIST OF FIGURES</b>	<b>x</b>
<b>LIST OF ABBREVIATIONS</b>	<b>xviii</b>
<b>LIST OF SYMBOLS</b>	<b>xx</b>
<b>ABSTRAK</b>	<b>xxii</b>
<b>ABSTRACT</b>	<b>xxiv</b>
<b>CHAPTER 1 : INTRODUCTION</b>	<b>1</b>
1.1 Research Background	1
1.2 High-Frequency Technology and its Applications	4
1.3 Nanoelectronic in High-Frequency Technology	8
1.4 State of the Art of Rectifying Devices	10
1.5 Problem Statement	12
1.6 Objectives	14
1.7 Research Scopes	14
1.8 Thesis Organization	16
<b>CHAPTER 2 : LITERATURE REVIEW</b>	<b>18</b>
2.1 Introduction	18
2.2 Physics Background	18
2.2.1 Semiconductor Diode	18

2.2.2	Nonlinear Device Analysis	22
2.2.3	Zero-biased Voltage	25
2.3	Planar Device	26
2.3.1	Self-switching Diode (SSD)	27
2.3.2	Geometric Diode	33
2.3.3	Ballistic Rectifier	37
2.3.4	Bulk Unipolar Diode	39
2.3.4.1	Camel Diode	40
2.3.4.2	P-Plane Barrier Diode	41
2.3.4.3	Planar Doped Barrier Diode	42
2.3.4.4	Graded Band Gap Diode	43
2.3.5	Thermionic Emission Current	44
2.3.6	Analysis Properties by Simulation	45
2.3.6.1	Geometry	46
2.3.6.2	PBD with Non-ballistic Carrier Transport	46
2.3.6.3	Properties of Dielectric Materials	47
2.3.6.4	Temperature Dependent	47
2.4	SILVACO ATLAS	49
2.4.1	DevEdit	50
2.4.2	Athena	50
2.4.3	Deckbuild	51
2.4.4	Tonyplot	51
2.5	Device's Physical Model	52
2.5.1	Mobility	52
2.5.2	Recombination	54
2.5.2.1	Shockley-Read-Hall (SRH)	54
2.5.2.2	Auger	56

2.5.3	Carrier Statistics	56
2.6	Summary	57
<b>CHAPTER 3 : METHODOLOGY</b>		<b>59</b>
3.1	Introduction	59
3.2	Simulation Process Flow	60
3.2.1	Defining SSD and PBD model	62
3.2.2	Validation of Devices Model	63
3.2.3	Parameters used in SSD Device Simulation.	65
3.2.3.1	Frequency Response of SSD	66
3.2.4	Physical Structure and Operation of new PBD	67
3.2.4.1	Si as Substrate Material	69
3.2.4.2	Parameters used in new PBD Device Simulation.	70
3.2.4.3	Frequency Response	71
3.3	Summary	71
<b>CHAPTER 4 : RESULTS AND DISCUSSION</b>		<b>73</b>
4.1	Introduction	73
4.2	RF Rectification using SSD	74
4.2.1	Si-based SSD Analysis	75
4.2.2	Effect of Device Geometry on $I$ - $V$ Characteristic of Si-based SSD	79
4.2.3	Effect of Various Materials and Temperatures on Current-Voltage ( $I$ - $V$ ) Characteristic of Si-based SSD	84
4.2.4	Frequency Response of Si-based SSD	89
4.2.5	Summary of SSD	94
4.3	New Si-based PBD	95
4.3.1	Simulation of Funnel-shape Semiconductor Channel	96
4.3.2	Thermionic Emission Current	99

4.3.3	Effect on Rectification Performance of PBDs with Different Geometrical Structures	101
4.3.4	Effect on Rectification Performance of PBDs with Different Dielectric Materials	106
4.3.5	Frequency Response of PBD	112
4.3.6	Summary of PBD	117
4.4	Comparison of Analytical Performance with Different High-Frequency Planar Devices	118
<b>CHAPTER 5 : CONCLUSION AND RECOMMENDATIONS</b>		<b>120</b>
5.1	Thesis Conclusion	120
5.2	Recommendations for Future Works	122
<b>REFERENCES</b>	<b>124</b>	
<b>APPENDIXES</b>	<b>137</b>	

## LIST OF TABLES

NO.		PAGE
Table 1.1:	The high-frequency technology and some of its application.	1
Table 2.1:	Recent publications of SSD for high-frequency application.	32
Table 2.2:	Recent publication of geometric diode for high-frequency application.	36
Table 2.3:	Several publication of ballistic rectifier for high-frequency application.	38
Table 3.1:	Physical models of planar diode.	62
Table 3.2:	Geometry parameter used in SSD device simulations.	66
Table 3.3:	Semiconductor properties.	70
Table 4.1:	Comparison between simulation and theoretical for cut-off frequency of the p-type Si-based SSD.	94
Table 4.2:	Comparison of frequency performance with different structure and materials high-frequency planar devices.	119

## LIST OF FIGURES

NO.	PAGE
Figure 1.1: Number of transistors in Microprocessor Unit (MPU) with cost performance, cost of high speed performance and functionality per chip of unit devices from 2001 until 2019.	3
Figure 1.2: Number of transistor relative to the devices frequency until 2019.	3
Figure 1.3: The electromagnetic spectrum.	5
Figure 1.4: THz technologies and global market prediction for future generation.	7
Figure 1.5: Nanoscale representation of nanotechnology with various naturally occurring objects.	8
Figure 1.6: A melting point of GaN cylindrical nanoparticles with respect to its size of the particles.	10
Figure 2.1: $I$ - $V$ characteristic of semiconductor diode.	19
Figure 2.2: Semiconductor diode p-n junction. (a) P-N junction with forward bias. (b) P-N junction with reverse bias.	19
Figure 2.3: $I$ - $V$ characteristic of the SSD with turn-on voltage is greater than 0 V. The diode is in forward bias at $T = 4.2\text{K}$ .	25
Figure 2.4: A nonlinear $I$ - $V$ characteristic with zero-bias voltage.	26
Figure 2.5: The SSD structure	27
Figure 2.6: Basic operation of SSD. (a) A depletion region near the etched boundaries. Depending on the sign of the applied voltage $V$ , the effective channel width will increase (b) or reduce (c), resulting to the diode-like characteristics.	28

Figure 2.7: Potential energy profile along the SSD channel at with different bias voltage.	29
Figure 2.8: $I - V$ characteristics of two InGaAs/InP-based SSDs with different channel widths. (a) Channel widths = 80 nm. (b) Channel widths = 50 nm.	30
Figure 2.9: $I - V$ characteristics of different relative dielectric materials use as insulator in SSD device. (a) GaN as dielectric materials. (b) InGaAs as dielectric materials.	31
Figure 2.10: Inverse arrowhead geometric diode structure. (a) A top view structure (b) 3D structure.	34
Figure 2.11: A staircase structure shape to replace the inverse arrowhead shape in Figure 2.10 with $V_{bias}$ was applied to the left electrode of the device, meanwhile the other electrode was grounded.	35
Figure 2.12: Ballistic diode.	37
Figure 2.13: Potential barrier profile of a camel diode.	41
Figure 2.14: Potential barrier profile of a $p$ -plane diode.	42
Figure 2.15: Potential barrier profile of a PDBD.	43
Figure 2.16: Potential barrier profile of a graded band gap diode.	44
Figure 2.17: $I - V$ characteristic of SSD with different $T$ ranging from 20 K to 300 K.	48
Figure 2.18: ATLAS device simulator.	50
Figure 2.19: ATLAS capabilities.	52
Figure 3.1: Process flow of planar diode.	61

Figure 3.2: (a) A typical topview scanning electron microscope (SEM) image of a single SSD. Upper inset shows the cross-section of SSD perpendicular to the channel. Lower inset shows the large-scale view including contacts, ground and biasing electrode.(b)  $I$ - $V$  characteristic of the simulated Si-based SSD using ATLAS simulator compared with  $I$ - $V$  characteristic of the experimental result taken from. 64

Figure 3.3: Top view of a PBD which has two terminals with a funnel-shape p-type Si channel. The light (grey) areas are the depletion regions caused by the interface charges between the p-type Si and insulator (air). Parameter  $W$  and  $\theta$  are the width of the device channel at the neck of the funnel shape, and the angle of the funnel, respectively. In our simulation,  $W = 20$  nm, and  $\theta = 72^\circ$ . 67

Figure 3.4: Energy band diagram with respect to the dotted line in where  $E_c$  is the conduction band energy and  $E_v$  is the valence band energy. The movement of holes has to overcome a higher energy barrier at reverse bias than forward bias due to asymmetrical energy barrier profile across the device channel. In both polarities, the device is expected to have an exponential characteristic over a certain current range. Note: Holes as majority carriers. 68

Figure 4.1: (a) Hole concentration profile for  $V_{bias} = 5$  V to  $-5$  V. Contour plot of hole concentration at (b)  $V = 0$  V, (c)  $V = 5$  V and (d)  $V = -5$  V. Note: The dotted lines show the cross-section at which the hole concentration profile is taken. 76

Figure 4.2:  $I$ - $V$  characteristic of the simulated Si-based SSD using ATLAS simulator with  $W = 230$  nm and  $L = 1.3$   $\mu$ m. 77

Figure 4.3: (a) Potential energy along the channel of the SSD with  $W = 230$  nm and  $L = 1.3$   $\mu$ m for  $V_{bias} = -5$  V, 0V and 5 V. A potential energy barrier reaches a value of  $\sim 0.52374$  eV for 0 V. (b) The large scale

view for  $V_{bias} = -5$  V, the holes flowing through a potential energy barrier along the channel of  $H = \sim 0.08727$  eV. Contrastly, almost no potential energy barrier under a forward bias.

78

Figure 4.4: (a)–(b)  $I$ - $V$  characteristics of SSDs with different  $W$  at  $L = 1.3$   $\mu\text{m}$  and  $W_t = 200$  nm, with the respected values of  $\gamma$ . Note that the dashed arrow in the  $I$ - $V$  characteristic graph indicates the changes in direction of the current as the geometry parameter of the device increases.

80

Figure 4.5: (a)–(b)  $I$ - $V$  characteristics of SSDs with different  $L$  at  $W = 230$  nm and  $W_t = 200$  nm, with the respected values of  $\gamma$ . Note that the dashed arrow in the  $I$ - $V$  characteristic indicates the changes in direction of the current as the  $L$  increases.

81

Figure 4.6: (a)–(b)  $I$ - $V$  characteristics of SSDs with different  $W_t$  at  $L = 1.3$   $\mu\text{m}$  and  $W = 230$  nm, with the respected values of  $\gamma$ . Note that the dashed arrow in the  $I$ - $V$  characteristic indicates the changes in direction of the current as the  $W_t$  increases.

83

Figure 4.7: (a)  $I$ - $V$  characteristic of SSDs with different  $\mathcal{E}_r$  at  $T = 300$  K,  $W = 230$  nm,  $L = 1.3$   $\mu\text{m}$  and  $W_t = 200$  nm. (b) The rectification performance of SSDs for temperature,  $T = 300$  K.

85

Figure 4.8: (a)  $I$ - $V$  curve for different temperature,  $T = 250$  K to 500 K. (b) The threshold voltage,  $V_{th}$  decreases as temperature increases. Note: Air as a relative dielectric permittivity.

86

Figure 4.9: The rectification performance of SSDs with different  $T$  and  $\mathcal{E}_r$  at  $W = 230$  nm,  $L = 1.3$   $\mu\text{m}$  and  $W_t = 200$  nm for temperature (a)  $T = 250$  K, (b)  $T = 300$  K, (c)  $T = 400$  K and (d)  $T = 500$  K.

87

Figure 4.10: The rectification performance of SSDs at  $T$  ranging from 250 K to 500 K with different  $\mathcal{E}_r$  at  $W = 230$  nm,  $L = 1.3$   $\mu\text{m}$  and  $W_t = 200$  nm. Note that the performance of SSDs decrease as temperature increases for all relative permittivity. 88

Figure 4.11:  $I$ - $V$  characteristics of SSDs with different  $L$  at  $W_t = 10$  nm and  $W = 230$  nm. The different  $L$  relevant for different value of the cut-off frequency of the rectifying behavior of SSDs. Note that the dashed arrow in the  $I$ - $V$  characteristic graph indicates the changes in direction of the current as the  $L$  increases. 89

Figure 4.12: Current response to the sinusoidal input voltage signals with amplitude of 1.0 V and frequencies of 1 GHz, 3 GHz and 10 GHz applied to the SSDs with  $W = 230$  nm,  $W_t = 10$  nm and  $L$  from 0.5  $\mu\text{m}$  to 1.3  $\mu\text{m}$ . Note that  $T$  is the period corresponded to the frequencies of the input voltage signals. 91

Figure 4.13: Mean output current with respect to the frequency of periodic input voltage with amplitude of 1.0 V, applied to the SSDs with  $W = 230$  nm,  $W_t = 10$  nm and  $L$  from 0.5  $\mu\text{m}$  to 1.3  $\mu\text{m}$ . The intrinsic cut-off frequency of the p-type Si-based SSD was  $\sim 19$  GHz. 92

Figure 4.14: A top view image of SSDs connected in parallel with  $L = 0.5$   $\mu\text{m}$  to 1.3  $\mu\text{m}$ ,  $D = 0.55$   $\mu\text{m}$  and  $t_{etch} = 10$  nm. Below right inset shows the top view image of a single SSD including biasing electrode and ground. Below left inset shows the cross-section of SSD perpendicular to the channel with vertical width,  $W_v$  of the device  $\sim 1$   $\mu\text{m}$ . 93

- Figure 4.15: (a)  $I$ - $V$  characteristic of the PBD with  $W = 20$  nm and  $\theta = 72^\circ$ . The turn-on voltage was  $\sim 0.6$  V. (b) Profile of the potential energy along the PBD channel at the neck of the funnel shape with  $W = 20$  nm and  $\theta = 72^\circ$  for  $V = -1.0$  V,  $0.0$  V and  $+1.0$  V. At zero bias, energy barrier of  $\sim 0.336$  eV with asymmetrical profile was formed. The majority carriers (holes) have to overcome energy barrier of  $\sim 0.042$  eV and  $\sim 0.047$  eV at forward and reverse bias, respectively. 97
- Figure 4.16: Contour plot of hole concentration at (a)  $V = 0$  V, (b)  $V = 1$  V and (c)  $V = -1$  V. (d) Hole concentration profile for  $V_{bias} = -1$  V to  $1$  V. Note: The dotted lines show the cross-section at which the hole concentration profile is taken. 98
- Figure 4.17:  $I$ - $V$  characteristic of the PBD with interface charge density ( $3.03 \times 10^{11}$  cm $^{-2}$ ). Graph showing  $I$ - $V$  characteristic based on simulation and thermionic theory. 100
- Figure 4.18:  $I$ - $V$  characteristic of the PBD with interface charge density ( $2.00 \times 10^{11}$  cm $^{-2}$ ). Graph showing  $I$ - $V$  characteristic based on simulation and thermionic theory. 101
- Figure 4.19: (a)  $I$ - $V$  characteristics based on funnel-shape semiconductor channel with different  $W$  at  $\theta = 72^\circ$ . Narrower  $W$  resists the reverse current more effectively. (b) Potential energy profile along the PBDs channel at  $\theta = 72^\circ$  and applied  $V = 1$  V with  $W = 10$  nm,  $20$  nm and  $30$  nm. Narrow channel width offer a higher energy barrier. 103
- Figure 4.20: The rectification performance of different  $W$  at temperature  $300$  K. Hence, more current flow at reverse current partly contributes to a low rectification performance. 104

- Figure 4.21: (a)  $I$ - $V$  characteristics of PBDs with different  $\theta$  ( $45^\circ$ ,  $63^\circ$ , and  $72^\circ$ ) for a fixed  $W$  of 20 nm. Upper insert show the large scale view for  $\theta = 45^\circ$  and  $63^\circ$ . For large  $\theta$  value, more forward current flowing through the funnel-shape channel is about  $\sim 6 \mu\text{A}$  and  $\sim 0.6 \mu\text{A}$  and  $\sim 15 \text{ nA}$  for  $\theta = 45^\circ$  and  $63^\circ$  respectively. (b) Potential energy profile along the PBDs channel at  $W = 20 \text{ nm}$  and applied  $V = 1 \text{ V}$  with different  $\theta$ . 105
- Figure 4.22: The rectification performance of PBDs with different  $\theta$  at  $W = 20 \text{ nm}$  for temperature 300 K. 106
- Figure 4.23:  $I$ - $V$  characteristic of PBDs with different  $\epsilon_r$  at  $T = 300 \text{ K}$ ,  $W = 20 \text{ nm}$  and  $\theta = 72^\circ$ . Note that the values of interface charge density and carrier density were fixed  $3.03 \times 10^{11} \text{ cm}^{-2}$  and  $2.45 \times 10^{16} \text{ cm}^{-3}$  respectively. 107
- Figure 4.24: (a) Potential energy profile along the PBDs channel at the  $W = 20 \text{ nm}$  and  $\theta = 72^\circ$  with applied  $V = 1 \text{ V}$ . (b) Enlarge scale view for Potential energy profile. High dielectric permittivity ( $\text{Al}_2\text{O}_3$ ) offer a lower energy barrier of  $\sim 0.027$ . 108
- Figure 4.25: The rectification performance of PBDs with different  $\epsilon_r$  at  $W = 20 \text{ nm}$  and  $\theta = 45^\circ$  for temperature 300 K. The lower  $\epsilon_r$  has a higher rectification performance at  $\sim 23 \text{ V}^{-1}$ . 109
- Figure 4.26: Rectification performance of PBDs with different  $T$  and  $\epsilon_r$ . (a)  $T = 250 \text{ K}$  (b)  $T = 300 \text{ K}$  (c)  $T = 400 \text{ K}$  and (d)  $T = 500 \text{ K}$ . 110
- Figure 4.27: Rectification performance of PBDs at  $T$  ranging from 250 K to 500 K. Note that the performance of PBDs decrease as temperature increases for all relative permittivity. 111

Figure 4.28: Current response to the sinusoidal input voltage signals with different  $W$  and  $\theta = 72^\circ$  at frequencies of (a) 1 GHz, (b) 10 GHz and (c) 50 GHz. Note that  $T$  is the period corresponded to the frequencies of the input voltage signals. 113

Figure 4.29: Mean output current with respect to the frequency of periodic input voltage with different  $W$  and  $\theta = 72^\circ$  at amplitude of 1.0 V, applied to PBDs device. The intrinsic cut-off frequency of the p-type Si-based PBDs with funnel-shape channel was  $\sim 1.1$  THz at  $W = 30$  nm. 115

Figure 4.30: Mean output current with respect to the frequency of periodic input voltage with different angle,  $W = 20$  nm at amplitude of 1.0 V, applied to PBDs device. The intrinsic cut-off frequency of the p-type Si-based PBDs with funnel-shape channel was  $\sim 0.8$  THz at  $72^\circ$ . 115

Figure 4.31: Mean output current with respect to the frequency of periodic input voltage with different relative dielectric permittivity,  $W = 20$  nm and  $\theta = 72^\circ$  at amplitude of 1.0 V, applied to PBDs device. The intrinsic cut-off frequency of the p-type Si-based PBDs with funnel-shape channel was  $\sim 0.8$  THz at Air as relative dielectric permittivity. 116

## LIST OF ABBREVIATIONS

1D	One-dimensional
2 DEG	Two-dimension electron gas
3D	Three-dimensional
AC	Alternating Current
Al <sub>2</sub> O <sub>3</sub>	Aluminium Oxide
AlGaN	Aluminium Gallium Nitride
AlGaSb	Aluminium Gallium Antimony
AUG	Auger recombination model
BJT	Bipolar Junction Transistor
BUD	Bulk Unipolar Diode
CONSRH	Concentration dependent lifetimes SRH
DC	Direct Current
EHF	Extremely High Frequency
EMF	Electromagnetic Field
ERCs	Explosives and Related Compounds
ETRAP	Specifies the trap energy of SRH recombination
FET	Field-effect Transistor
FLDMOB	Parallel electric field dependent
GaAs	Gallium Arsenide
GD	Geometric Diode
GaN	Gallium Nitride
GNRs	Graphene Nanoribbons
GPS	Global Positioning System
HBT	Heterojunction Bipolar Transistor
HF	High-Frequency
InAlAs	Indium Aluminium Arsenide
InAs	Indium Arsenide
InGaAS	Indium Gallium Arsenide
InP	Indium Phosphide
IR	Infrared
ITRS	International Technology Roadmap for Semiconductor
<i>I-V</i>	Current-Voltage
LAN	Local Area Network

LED	Light Emitting Diode
MC	Morte Carlo
MISFET	Metal Insulator Semiconductor Field Effect Transistor
MOS	Metal Oxide Semiconductor
MPU	Microprocessor Unit
PBD	Planar Barrier Diode
PDA	Personal Digital Assistant
PDBD	Planar-doped Barrier Diode
RF	Radio Frequency
RFID	RF Identification
SHF	Super High Frequency
Si	Silicon
SiC	Silicon Carbide
SiGe	Silicon Germanium
SiO <sub>2</sub>	Silicon Dioxide
SLG	Single Layer Graphene
SRH	Shockley-Read-Hall
SSD	Self-switching Diode
TAUN0	Specifies SRH lifetime for electron
TAUP0	Specifies SRH lifetime for hole
TB	Triangular shape
TCAD	Technology Computer Aided Design
TSS	Tangential Signal Sensitivity
UHF	Ultra High Frequency
VHF	Very High Frequency
WiFi	Wireless Fidelity
ZnO	Zinc Oxide

## LIST OF SYMBOLS

$\Delta i$	Identical to the first bracket term on the right-hand side
$\psi$	Electrostatic potential
$\theta$	Angle
$\gamma$	Curvature coefficient
$\phi_{BL}$	Potential barrier height for the carrier to move from left
$\phi_{BR}$	potential barrier height for the carrier to move from right
$A^*$	Effective Richardson constant for electron
$\text{\AA}$	Amstrong
$C$	Capacitance
$C_{jo}$	Junction capacitance at zero bias
$C_p$	Parasitic capacitance
$\epsilon_0$	Permittivity of free space
$\epsilon_g$	Bandgap
$\epsilon_r$	Dielectric permittivity
$E$	Electric field
$eV$	Electron volt
$f$	Frequency
$f_{max}$	Frequency maximum
$f_t$	Cutoff frequency
$f^{(N)}$	$N^{th}$ order derivative of $f(V)$
GHz	Gigahertz
H	Potential energy inside the channel
Hz	Hertz
$I_s$	Total current density
$J$	Reverse saturation current
K	Kelvin
k	Boltzman constant
kHz	KiloHertz
L	Channel length
MHz	Megahertz
MUN	Electron mobilities
$N$	Carrier density
nm	Nanometer

$\rho$	Local space charge density
$q$	Magnitude of electrical charge of an electron
$R_D$	Differential resistance
$R_s$	Series resistance
$t$	Timeline
$\mu$	Electron mobility
$\mu_{no}$	Low field electron mobility
$\tau_n$	Electron lifetime
$\tau_p$	Hole lifetime
T	Terahertz
$T_L$	Lattice temperature
THz	Absolute temperature
$\mu\text{m}$	Micrometer
$\mu\text{A}$	Micro ampere
V	Voltage across the diode
$V_{\text{bias}}$	Applied bias voltage
$V_D$	Applied voltage
$V_o$	Applied DC bias
$V_{\text{sat}}$	Electron saturation velocity
$V_{\text{TH}}$	Threshold voltage
$v_{RF}$	Frequency signal voltage
$\omega$	Angular frequency
W	Channel width
$W_t$	Trench width
$W_v$	SOI thickness
$X_C$	Capacitive reactance

## REKABENTUK DAN PENCIRIAN STRUKTUR DIOD PENSUISAN-SENDIRI DAN DIOD SAWAR SATAH SEBAGAI PENERUS BERKELAJUAN TINGGI

### ABSTRAK

Pembangunan peranti penerus berkelajuan tinggi telah menjadi salah satu bidang penyelidikan utama yang boleh digunakan dalam banyak aplikasi, termasuk frekuensi radio (RF) dan sistem pengesanan. Contoh-contoh peranti ini ialah diod Schottky dan diod sawar terdop-satah. Walau bagaimanapun, semua peranti yang sangat cemerlang ini memerlukan proses fabrikasi yang sangat mencabar disebabkan oleh struktur-struktur yang kompleks dan kepekatan pengedopan yang tepat untuk setiap lapisan kritikal yang mana kosnya adalah agak tinggi. Prospek menggunakan peranti-peranti elektronik dengan struktur satah telah menjadi semakin mempunyai harapan. Peranti-peranti planar ini memberi kelebihan tambahan bukan hanya mudah malah boleh juga beroperasi pada frekuensi tinggi. Oleh demikian, dalam kerja penyelidikan ini, kemungkinan penggunaan dua buah peranti nano satah berasaskan diod pensuisan-sendiri (SSD) dan diod sawar satah (PBD) untuk gelombang mikro dan penerusan terahertz telah ditunjukkan menggunakan penyelakuan. SSD telah ditunjukkan sebagai penerus suhu bilik yang beroperasi pada frekuensi terahertz. Dalam kerja penyelidikan ini, prestasi penerus SSD dinilai menggunakan parameter yang dikenali sebagai pekali kelengkungan, yang diperolehi daripada ciri-ciri arus-voltan ( $I-V$ ) peranti tersebut. Kesan mengubah struktur geometri dan dielektrik penebat nisbah kebertelusan (dari 1 - 9.3) sesuatu SSD keatas pekali kelengkungan peranti tersebut dikaji dan dianalisa dengan menggunakan alat penyelakuan dua dimensi. Penyelakuan juga dilakukan di bawah julat suhu 250 - 500 K. Hasilnya menunjukkan bahawa frekuensi potong tertinggi yang dicapai dalam kerja penyelidikan ini adalah menghampiri 19 GHz, beroperasi pada keadaan yang tidak terpinang. Dengan melaksanakan penyelakuan serupa yang digunakan dalam menunjukkan SSD berasaskan silikon, satu diod-nano satah ekakutub baharu sebagai satu penerus telah diperkenalkan dan dibangunkan dalam kerja penyelidikan ini. Peranti baru ini dirujuk sebagai PBD yang mempunyai satu saluran geometri bentuk corong yang membolehkan arus mengalir merentasi peranti. Pada pincang sifar, kawasan susutan yang tidak seragam, telah terjadi pada bahagian leher saluran bentuk corong disebabkan oleh cas permukaan pada antara muka semikonduktor/ penebat, diramalkan untuk mencipta sawar tenaga di sepanjang saluran dengan profil yang tidak simetri. Voltan luaran yang digunakan merentasi satu PBD dijangka akan menghasilkan ketinggian yang berbeza sawar tenaga bergantung sama ada voltan yang diberikan adalah positif atau negatif. Hasilnya, ciri-ciri  $I-V$  tak lurus direalisasikan yang mana boleh digunakan dalam penerusan isyarat. Prinsip operasi PBD ini telah ditunjukkan dan disahkan dalam penyelakuan kerja penyelidikan ini. Ia juga telah diterangkan dengan menggunakan teori pemancaran ion haba yang boleh mengawal aliran arus merentasi peranti. Serupa dengan SSD, prestasi penerusan PBD telah dicirikan dan dinilai berdasarkan pekali kelengkungan dan frekuensi potong peranti tersebut. Dengan mengubah rekabentuk geometri dan nisbah dielektrik penebat kebertelusan (dari 1-9.3) PBD, pekali kelengkungan peranti boleh dioptimumkan untuk meningkatkan prestasi penerus. Frekuensi potong tertinggi yang diperolehi dalam

penyelakuan kerja penyelidikan ini adalah menghampiri 0.8 THz. Kedua-dua peranti SSD dan PBD ini mempunyai senibina sawar yang seterusnya boleh direalisasikan dengan satu langkah litografi yang akan menjadikan keseluruhan proses fabrikasi peranti lebih mudah, lebih cepat dan lebih murah jika dibandingkan dengan peranti elektronik konvensional yang lain.

©This item is protected by original copyright

## DESIGN AND CHARACTERIZATION OF SELF-SWITCHING DIODE AND PLANAR BARRIER DIODE AS HIGH-FREQUENCY RECTIFIERS

### ABSTRACT

The development of high-speed rectifying devices has become one of major research areas which can be utilized in many applications, including radio-frequency (RF) and detection systems. Examples of these devices are Schottky diode and planar-doped barrier diode. However, all these excellent devices require a very challenging in fabrication process due to their complex structures and a precise doping concentration for each critical layers which are relatively high cost. The prospects of using electronic devices with planar structure are therefore become increasingly promising. These planar devices provide additional advantages of being not only simple but also able to operate at high frequencies. As such, in this research work, the feasibility of utilizing two silicon-based planar nanodevices of self-switching diode (SSD) and planar barrier diode (PBD) for microwave and terahertz rectification has been demonstrated using simulations. SSD has recently been demonstrated as room-temperature rectifiers operating at terahertz frequencies. In this research work, the rectifying performance of SSD is evaluated using a parameter known as the curvature coefficient, derived from the current-voltage ( $I$ - $V$ ) characteristic of the device. The effects of varying the geometrical structure and the insulator dielectric relative permittivity (from 1 – 9.3) of SSD on the curvature coefficient of the device are studied and analyzed by means of a two-dimensional device simulator. The simulations are also performed under temperature range of 250 – 500 K. The results show that the highest cut-off frequency attained in this research work is approximately 19 GHz, operating at unbiased condition. By implementing similar simulation settings used in demonstrating silicon-based SSDs, a new unipolar planar nanodiode as a rectifier is introduced and developed in this research work. This new device is referred as PBD which has a funnel-shaped geometrical channel that allows current to flow across the device. At zero bias, the nonuniform depletion region, developed at the neck of the funnel-shape channel due to surface charges at semiconductor/insulator interface, is predicted to create an energy barrier along the channel with asymmetrical profile. An external voltage applied across a PBD is expected to produce different height of the energy barrier depending either the voltage given is positive or negative. As a result, a nonlinear  $I$ - $V$  characteristic is realized which can be utilized in signal rectification. This operating principle of PBD has been demonstrated and validated in the simulations of this research work. It has also been described using thermionic emission theory which may govern the flow of current across the device. Similar to SSD, the rectification performance of PBD is characterized and evaluated based on the curvature coefficient and cut-off frequency of the device. By varying the geometrical design and insulator dielectric relative permittivity (from 1-9.3) of PBD, curvature coefficient of the device can be optimized in order to improve the rectification performance. The highest cut-off frequency obtained in the simulation of this work is approximately 0.8 THz. Both SSD and PBD have a planar architecture that can therefore be realized in a single lithography step which makes the whole fabrication process of the devices simpler, faster and at lower cost when compared with other conventional electronic devices.