

Speed and Area Efficient FXP Adders and Multipliers: A Comparative Analysis for LNS System

Abstract

In this paper, a variety of adder and multiplier are compared to be implemented in a new logarithmic number system (LNS). Both adder and multiplier are designed with a generic very high-speed integrated circuit hardware description language (Verilog) program. This makes it possible to achieve the optimum performance in latency and area of 0.18 μ m CMOS technologies LNS chip. Consequently, the optimal configurations vary with speed and area of the schemes and in some cases can be compact area, $O(n)$, fast in latency $O(\log_2 n)$ or optimized. The program was scripted based on fixed-point (FXP) adders and multipliers that yet will be implemented in LNS system. The functionality of the scheme was tested before synthesized. Outcomes show that Ladner Fisher (LF) adder and modified Baugh Wooley multiplier contribute to fast in latency and consume minimal area.