Conference Proceedings – Volume 932, Issue 1, IOP Conference Series: Materials Science and Engineering 2020, Pages 1 - 12

Hybrid Floating Point/Logarithmic Number System Processor

Abstract

Hybrid Floating Point/Logarithmic Number System processor is an Arithmetic Logic Unit with hybrid architecture in which its data computation involves Floating Point (FLP) and Logarithmic Number System (LNS). LNS processor has high performance but requires complicated hardware to support its function, especially LNS addition and subtraction. Therefore, hybrid processor is proposed to perform multiplication/division in LNS, addition/subtraction in FLP. Through merging FLP and LNS, data computation can be done in a faster, precise and less complicated way. The proposed research is a 32-bit Hybrid FLP/LNS processor, which involving 32-bit fixed point data format and 32-bit single precision FLP format. The EDA tools used in developing and simulating this project is based on Synopsys Design Compiler and Altera Quartus II, and the Hardware Description Language used is Verilog HDL. Logical synthesis of this project is done by using Synopsys Design Compiler and its area, timing and power are validated.