Journal of Physics:
Conference Series

PAPER • **OPEN ACCESS**

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To cite this article: F Fauzi *et al* 2023 *J. Phys.: Conf. Ser.* **2550** 012024

Dual Outputs Switch Mode Power Supply (DOSMPS) Utilizing Forward Converter Topology

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Abstract. Experimental works of dual, 5 volt DC outputs switch mode power supply (DOSMPS) is presented in this paper. To design, construct and evaluate the DOSMPS using forward converter topology are the objectives of this article. In this work, a 556 timer was picked as the pulse width modulator. The 556 timer was picked because it is widely used, cheap and capable of producing stable dual pulse width modulations. Since, this work targeted dual DC outputs, two forward converter circuits were built. However, switching frequencies at two transistors were controlled by only one 556 timer. The complete circuit of the DOSMPS consist of full bridge rectifier, smoothing capacitor, two high frequency transformers and two forward converter circuits. At the first stage of this work, the DOSMPS circuit was designed using Proteus software. Later, the complete DOSMPS circuit was constructed on two breadbroads after all of the electronic components and devices were available. Important parameters such as the input and output voltages and duty cycles were measured using digital oscilloscope and multimeter. Results from these measurements have shown that the designed circuit can convert single-phase 24 Vrms 50 Hz AC voltage input into dual and stable 5±0.1 V DC outputs. Also from this work, it was observed that, pulsed DC voltages with peak value of 2 V and frequency less than 20 kHz are sufficient in controlling the switching frequencies of both BJT transistors. This allows the regulation of the output voltage within the desired range. Analysis carried out after the measurements has shown close correlation between the theoretical and experimental results, where the calculated and measured switching frequencies had only deviated by 1.1%.

Keywords: Forward converter, 556 timer, dual output switch mode power supply

1. Introduction

In switch mode power supply, switching mechanism plays a very important role in conversion of DC or AC voltages to a desired DC voltage level. The advantages of SMPS compared to linear power supply are, its compact size and lightweight. Omitting the low frequency transformer in the SMPS design is one of the prerequisite, to achieve the lightweight and compactness of SMPS [1]. In SMPS circuits, the heavy and bulky low frequency transformer is substituted with high frequency, ferrite core transformer. However, high frequency switching circuit operated at kilo hertz frequency or higher is compulsory due to the presence of the ferrite core transformer. Without the high frequency, pulsed DC voltage signal, stepping-up or steeping-down voltage of the primary side could not be realized. So pulse width modulation is necessary in order to regulate the output voltage within the targeted level.

In this project, 556 timer was employed as the pulse width modulator. The 556 timer is an integrated circuit (IC) that shares many similarities with 555 timer that has been designed in 1971 [2]. In contrast to the 555 timer which is an 8 pins IC, the 556 timer has 14 pins. The 14 pins architecture enables the 556 timer to have two output pins.

Forward converter is a well known topology that has been used in switch mode power supplies. Research in forward converters includes switch modelling, power factor improvement and soft-switching technique [3-5]. In this project, forward converter was employed at the secondary side of the transformer to produce dual 5 volt DC voltages. Forward converter is one of the isolated DC-DC converters [6]. One of the advantages of forward converter is, it can keep the output current nearly constant and this is more preferable for high output current application [7].

For this project, initial works involving the design and computer simulations were conducted using electrical circuit design software, Proteus. The construction and assembly of electronics components were carried out after results obtained from the computer simulation were satisfactory. The input voltage has been lowered to 24 Vrms 50 Hz AC from the normal 240 Vrms 50 Hz AC. The 240 Vrms 50 Hz was lowered using GW Instek APS-9301 power supply unit.

All of the required components and devices were attached on two breadboards. Digital oscilloscope (Tektronix TPS 2014) and multimeter (GW Instek GMD391) were utilized to measure important parameters such as input and output voltages, duty cyles and others.

2. Methodology

Figure 1 shows the complete circuit designed with Proteus software. The AC voltage input is rectified at full bridge rectifier. The four diodes used for the bridge rectifier are from 1N4007 type. A smoothing capacitor, C_3 with the capacitance of 100 µF can be seen across the full bridge rectifier. Two resistors next to C_3 are used as voltage divider to lower the smoothed DC voltage, before channelling it to 556 timer. In Proteus software, 556 timer as a single IC was not available in the library. Alternatively, two 556 timers (U1A & U1B) were used as substitute.

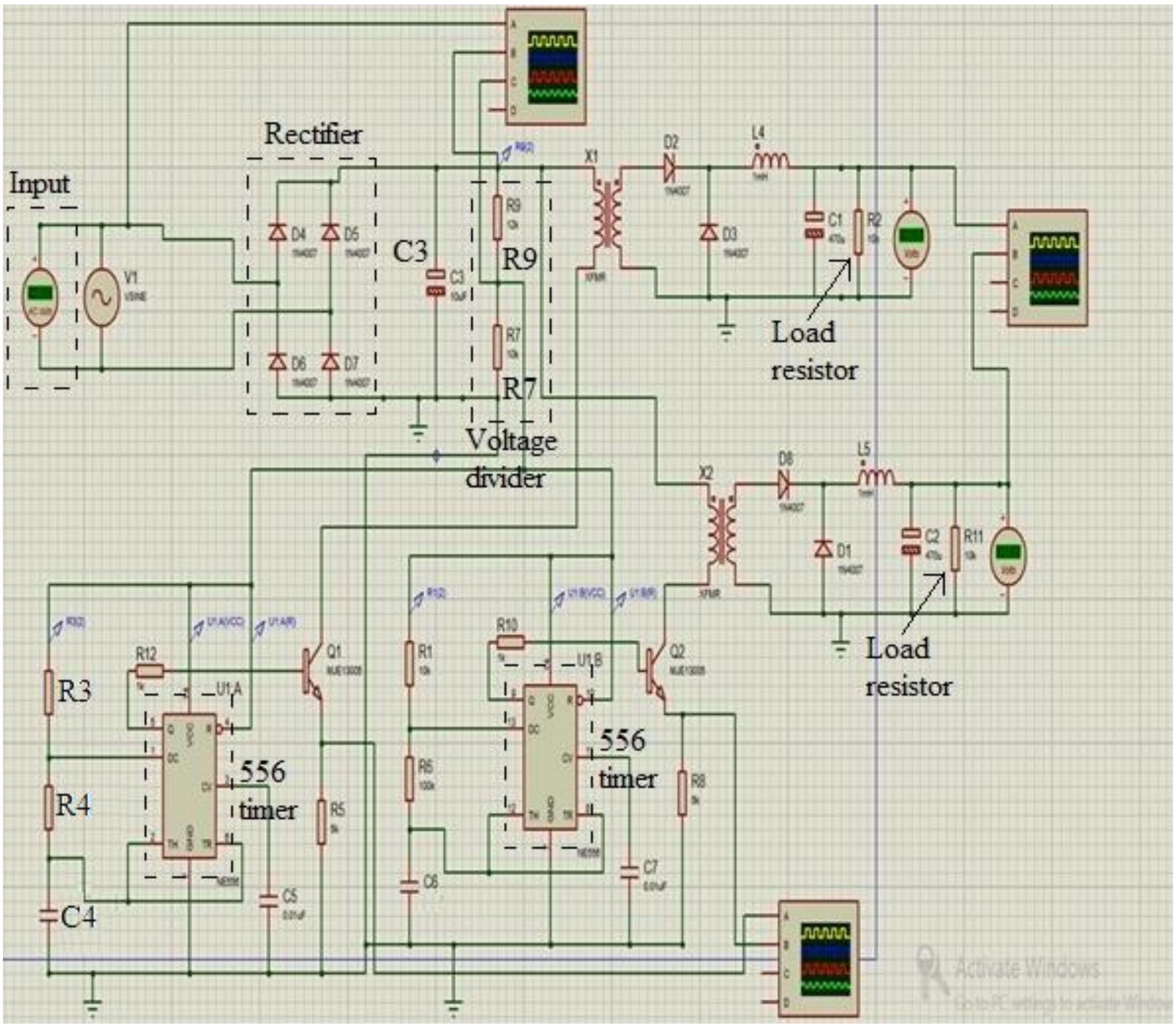

Figure 1. Circuit of DOSMPS with forward converter topology designed with Proteus software

The value of resistors next to C_3 are R_9 = 12 000 Ω and R_7 = 10 000 Ω respectively. The 556 timer can accommodate DC voltage from 6 ~ 18 V. The input voltage (V_{cc}) to the 555 timer is determined as:

$$Vcc = \frac{(R_7)(24\times\sqrt{2}-1.4)}{R_7+R_9} \quad (2.1)$$
$$= 14.81 \text{ V}$$

The time taken, t_H for the 390 pF capacitor (C_4) to charge up to 0.67V_{cc} [8]:

$$t_H = (0.694)(R_3+R_4)(C_4) \quad (2.2)$$
$$= (0.694)\ (10\ 000\ \Omega + 100\ 000\ \Omega)\ (C_4)$$
$$= 29.77\ \mu\text{s}$$

Conversely, t_L is the time for capacitor C_4 to discharge to 0.13V_{cc}:

$$t_L = (0.694)(R_4)(C_4) \quad (2.3)$$
$$= (0.694)\ (100\ 000\ \Omega)\ (C_4)$$
$$= 27.07\ \mu\text{s}$$

The frequency of the pulsed DC voltage at the output pins of the 556 timer:

$$f = \frac{1}{t_H+t_L} \quad (2.4)$$
$$= 17{,}593.24 \text{ Hz}$$

So, the duty cycle, D:

$$D = \frac{29.77\ \mu\text{s}}{29.77\ \mu\text{s} + 27.07\ \mu\text{s}}\times 100 \quad (2.5)$$
$$= 52.37\ \%$$

The pulsed DC voltages is directed to the gates of MJE13005 BJT transistors. After the BJT transistors, there are two ferrite core transformers (one for each forward converters), which used to step down the smoothed DC voltage. The inner and outer diameters of the ferrite core transformer are 1.2 and 1.5 cm respectively. Looking from secondary side of the transformer, the capacitance of C_1 and C_2 is 470 x 10^{-6} F and the load resistor is a 10 000 **Ω**. The four diodes used at the forward converter circuits are also from the 1N4007 type.

The targeted DC output voltage at the load resistor is 5 volt and the transformer ratio, n is determined as:

$$n = \frac{N\text{s}}{N\text{p}} = \frac{V\text{s}}{DV\text{p}} \quad (2.6)$$
$$= \frac{(5+0.7)\text{ V}}{(0.52)(33.94\text{ V})}$$
$$= 0.32$$

The transformer ratio, 0.32 was used in the beginning. All components shown earlier in **Figure 1** have been included on the two-separate breadboards and can be seen in **Figure 2.** Next section will present the measurement result of important parameters for this project.

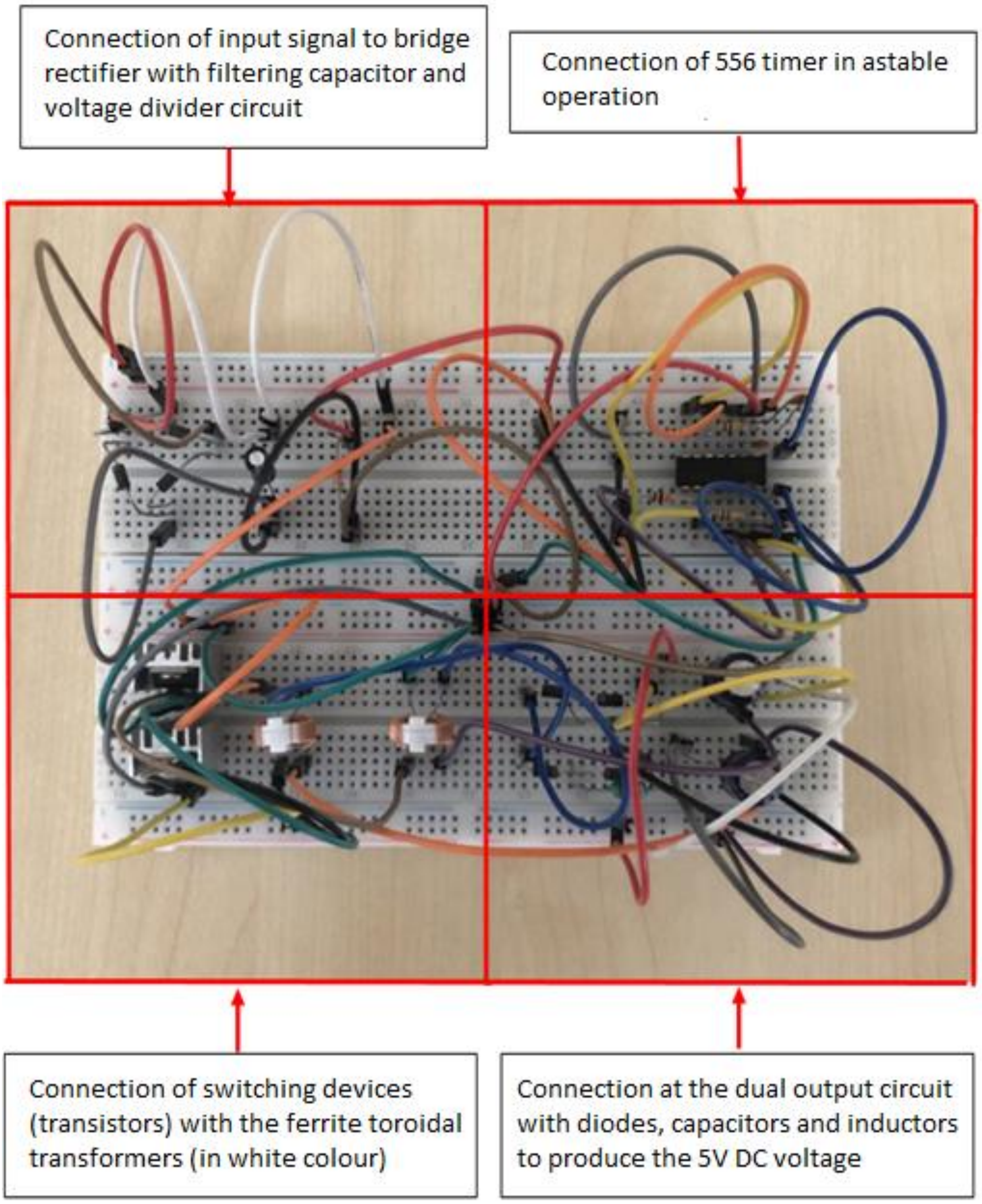

Figure 2. The complete hardware circuit of DOSMPS circuit built on two breadboards

3. Results and Discussion

Figure 3 shows the output voltage from the full bridge rectifier. In this figure, the peak value observed from the Tektronix TPS 2014 digital oscilloscope is around 32 V. This value is acceptable since 24 V_{rms} was used as the input to the full bridge rectifier.

 2550 (2023) 012024 doi:10.1088/1742-6596/2550/1/012024

Figure 3. The output voltage from full bridge rectifier showing peak about 32 V

The inclusion of 10 µF smoothing capacitor across the full bridge rectifier has straighten the waveform in **Figure 4.** Measurement of the 'straight' DC voltage using a multimeter has shown the value of 32.23 V.

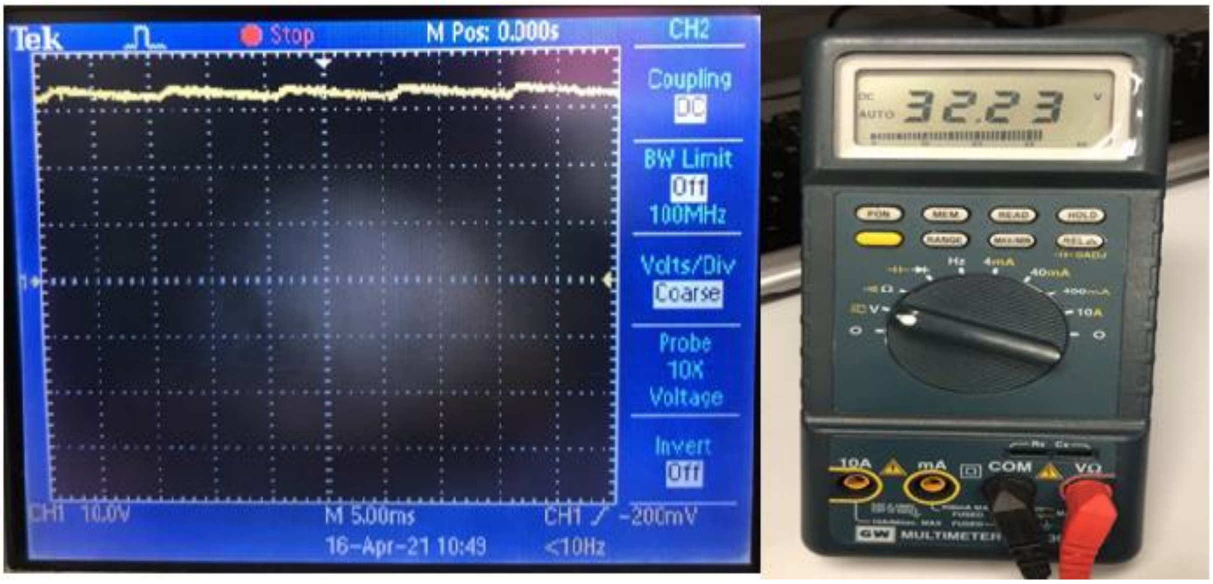

Figure 4. The 'straight' DC voltage after being smoothen by a 10 µF capacitor.

By referring back to **Figure 1**, it is clear that the voltage in **Figure 4** will be channeled to the voltage divider. At here, the voltage will be decreased to be below 18 V because this is the upper limit accepted by the 556 timer. As being shown in **Figure 5**, the process of stepping down the 32 V voltage was successful. Now the voltage value at the input pins (V_{cc}) of the 556 timer has been reduced to 14.64 V as shown in **Figure 5.**

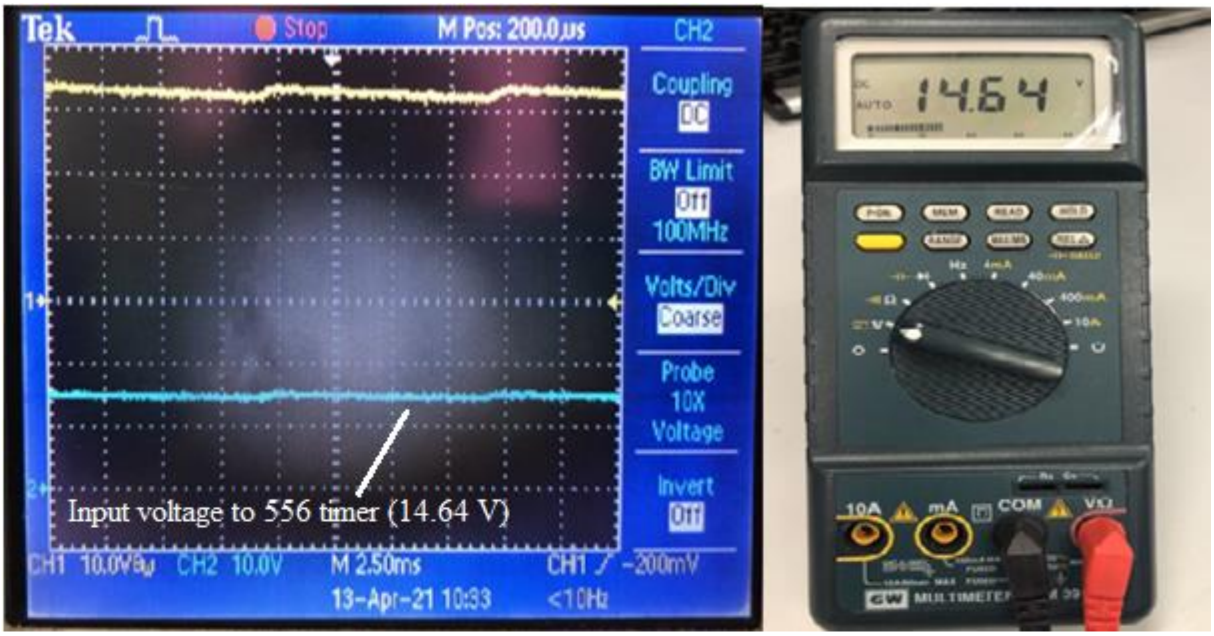

Figure 5. DC voltage being decreased to 14.64 V and later channeled to the V_{cc} pin of the 556 timer

The dual pulsed DC output voltages from 556 timer are shown in **Figure 6**. As shown in this figure, For the vertical axis, the measurement was set to 2 V per division. While for the horizontal axis, the scale was set to 25 µs per division. The peak values of the pulsed DC voltages is close to 2 V. This is sufficient to turn on the MJE13005 transistor according to the datasheet provided [9]. By observing the horizontal axis of the oscilloscope, one can see that the charging time (t_H) and discharging time (t_L) are 15 µs and 42.5 µs, respectively. So, the duty cycle is 0.26. This is 50% decrease from the calculated duty cycle. It is believed that the decrease of duty cycle can be related to existence of high impedance in the real circuit. It is worth to mention that circuit impedance's was not considered to determine the charging time, discharging time and duty cycles carried out before.

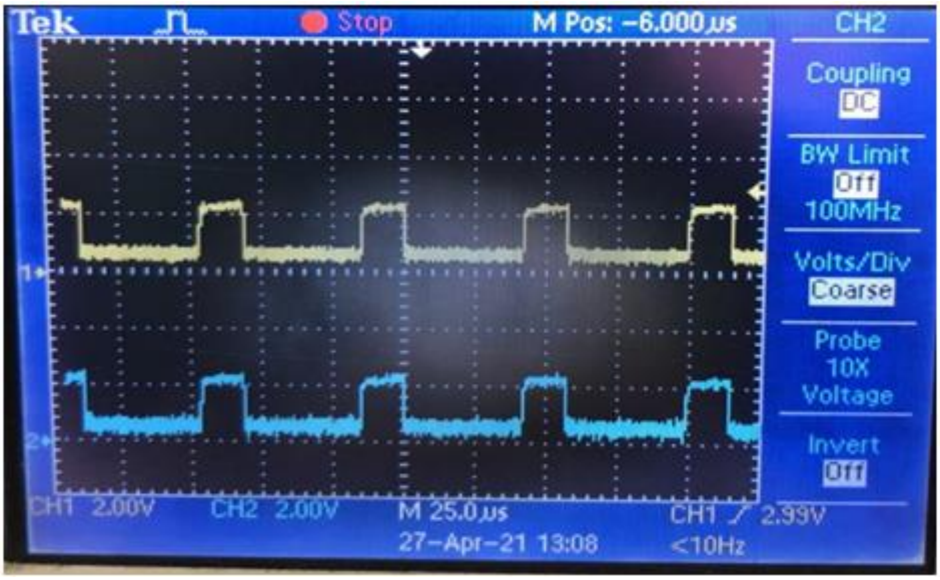

Figure 6. Dual pulsed DC voltage produced by 556 timer

Further adjustment of the transformer ratio was necessary to obtain the output voltages close to 5 volt. So after numerous trial, the transformer ratio was changed from 0.32 to 0.67. The number of turns at the primary and secondary side were reset to 20 and 14 respectively. The adjustment has successfully reduced the duty cycles from 0.52 to 0.26 as can be seen in **Figure 6**. Thus the new transformer ratio, *n* was recalculated as:

$$n = \frac{Ns}{Np} = \frac{Vs}{DVp} \tag{3.1}$$

$$= \frac{(4.93 + 0.7)\ \text{V}}{(0.26)(32.23\ \text{V})}$$

$$= 0.67$$

The adjustment of the transformer ratio, has proven successful because dual DC outputs close to 5 V can be observed from the oscilloscope (**Figure 7)**. Further measurement carried out using digital multimeter also confirm that the DC output voltage is 4.93 V (close to 5 V)

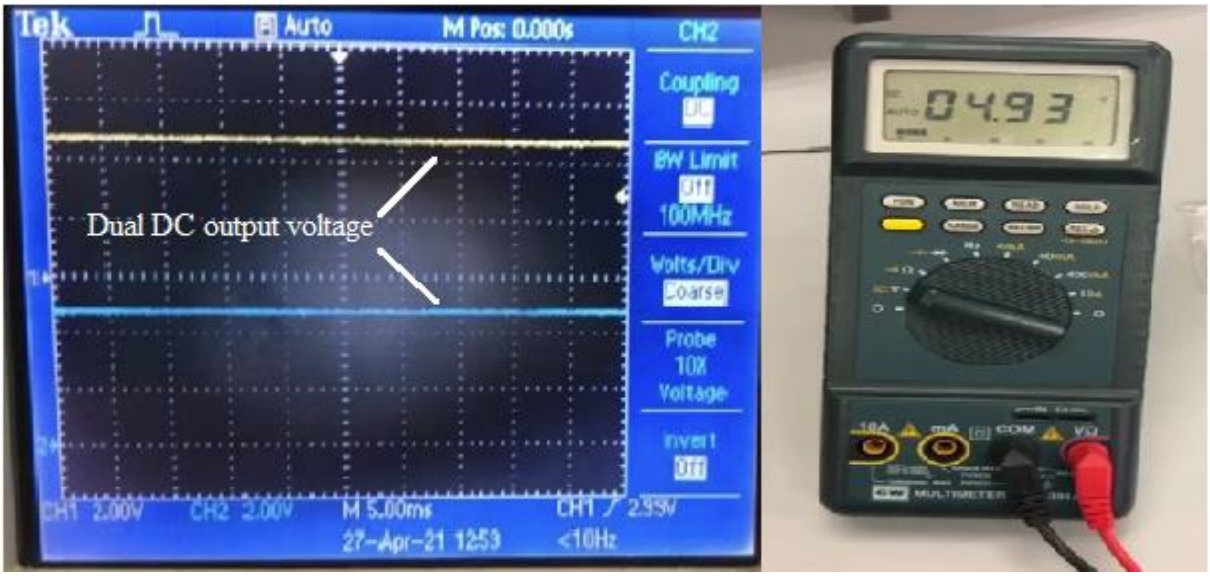

Figure 7. Output voltage at the load resistors measured using oscilloscope and digital multimeter

Additional analysis was carried out to see the accuracy between the theoretical and practical results. By looking at **Table 1**, it shows for the switching frequencies, the deviation of practical results is small if compared to the theoretical results. Deviation of switching frequencies for both theoretical and practical circuits was just only 1.10 %.

Table 1. Comparison between the theoretical and practical results

	Theoretical result	Practical result
Low output duration	$t_L = 27.07\mu s$	$t_L = 42.50\ \mu s$
High output duration	$t_H = 29.77\ \mu s$	$t_H = 15.00\ \mu s$
Period	$T = 56.84\ \mu s$	$T = 57.50\ us$
Frequency	$f = 17{,}593.24$ Hz	$f = 17{,}391.30$ Hz
Percentage of error with theoretical		$= \frac{17{,}593.24\ \text{Hz} - 17{,}391.30\ \text{Hz}}{17{,}593.24\ \text{Hz}} x\ 100$ $= 0.011\ x\ 100\%$ $= 1.10\%$
Duty cycle	$D = 0.52$ @ 52%	$D = 0.26$ @ 26%
Percentage of error with theoretical		$= \frac{0.52 - 0.26}{0.52} x100$ $= 50\%$

Comparatively, the deviation of duty cycles between the theoretical and practical results is huge. The calculation of duty cycles in section 2 was done without considering overall impedance of the circuit. The overall impedance in the real circuit caused the 50% mismatch between the theoretical and practical results as shown in **Table 1**. The existence of this impedance is also the main reason for the decrease in duty cycle from 0.52 to 0.26.

4. Conclusion

The objective of this project, which are to design, build and assess the DOSMPS with forward converter topology has been achieved. The designed circuit was proven to be successful because it has converted 24 Vrms 50 Hz input voltage into dually stable 5±0.10 V DC. The project started from the theoretical aspect where several important calculations were carried out to determine the important parameters of electronic components. Then the complete DOSMPS circuit was designed and simulated in Proteus software. Successful simulation works led to the construction, testing and measurement of real circuit.

This work also has shown that 556 timer is sufficient to be used as dual outputs pulse width modulator for the purpose of switching regulation in low power SMPS. The pulsed DC voltage from the timer with frequency of 17.4 kHz and peak value of 2 V was sufficient to turn on and off MJE13005 transistors. Additional analysis has shown that close correlation does exist between theoretical and practical results in term of the switching frequencies because the deviation just only 1.1%.

Incorporating the feedback loop can self-regulate the output voltage if unexpected errors occur. This is the next improvement that can be implemented for the future work.

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Acknowledgement

The authors would like to acknowledge the support from the Faculty of Electrical Engineering and Technology, Universiti Malaysia Perlis (UniMAP) for the FTKE Research Activities Fund.