A STUDY ON CRITICAL TO FUNCTIONAL PARAMETERS OF FLIP CHIP DIE BONDING TECHNOLOGY IN SEMICONDUCTOR INDUSTRIAL NEEDS

by

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LIST OF ABBREVIATIONS

IC	Integrated circuit
TC	Temperature cycle
PCT	Pressure cooker test
C4	Control collapsed chip connection
FC	Flip chip
TCB	Thermocompression bonding
RTS	Ramp to soak
RSS	Ramp soak spike
ACA	Anisotropic conductive adhesive
ICA	Isotropic conductive adhesive
ACF	Anisotropic conductive film
MEMS	Micro-Electro-Mechanical Systems
LED	Light emitting diode
HVM	High volume manufacturing
PCB	Printed circuit board
IMC	intermetallic compound
TAL	Time above liquid
mm	Millimetre
mN	Milinewton
I/O	Input output
LDV	Laser Doppler vibrometer
CCD	Charge couple device
ms	Millisecond
µm	Micrometre
kHz	Kilo hertz
cm	Centimetre
SEM	Scanning electron microscope
ENIG	Electroless nickel immersion gold
Al	Aluminium
mΩ	Milliohm
COG	chip on glass

Mpa	Mega Pascal
W	Watt
TCT	Thermal cycle test
ENEPIG	Electroless nickel electroless palladium immersion gold
OSP	Organic solder ability preservative
DIG	Direct Immersion Gold
IT	Immersion Tin
Pd	Palladium
Ni-P	Nickel Phosphorus
FPFCBGA	Fine pitch flip chip ball grid arrey
MRT	Mass reflow temperature
SPL	Single piece lid
EN(B)EPIG	electroless nickel-boron/electroless palladium/immersion gold
Cu OSP	Copper Organic Solder ability Preservative
SF6	sulphur hexafluoride
Zn	Zinc
Bi	Bismuth
UBM	Under bump metallization
Cr	Chromium
Ti	Titanium
W	Tungsten
TiW	Titanium tungsten
EDS	Energy Disperse Spectrum
ATC	Accelerated thermal cycling
ITO	Indium tin oxide
HTS	High temperature storage
HH	High humidity
HT	High temperature
TH	Temperature humidity
uHAST	Unbiased high accelerated stress test
MSL	Moisture sensitivity level

HAST	High accelerated stress level
TSV	Through silicon via
DRAM	Dynamic random access memory
BT	Bismaleimide triazine
EM	Electromigration
POB	particle on bump
EHDA	Electrohydrodynamic Atomization
ICB	Inclined conductive bump
UPH	Unit per hour
PMD	Pre and main divided
SMT	Surface mount technology
CFC	Condensation of perfluorocarbon
IR	Infrared
ASMp	ASM Pacific
BESI	BE semiconductor industries
SET	Smart Equipment Technology
FEA	Finite Element Analysis
FEM	Finite Element Modelling
CAD	Computer aided designing
3D	3 Dimension
BGA	Ball grid array
RAM	Random access memory
Fe_2O_3	Iron Oxide
SiO_2	Silicon dioxide
Al_2O_3	Aluminum oxide
SnPb	Tin Lead
SLR	Systematic literature review

LIST OF SYMBOLS

°C	Celsius
%	Percentage
wt%	Percentage by weight
°C/s	Celsius per second
K/s	Kelvin per second
N	Newton
ppm	parts per million

KAJIAN MENGENAI PARAMETER KEFUNGSIAN YANG KRITIKAL BAGI TEKNOLOGI DIE BONDING UNTUK KEPERLUAN PERINDUSTRIAN SEMIKONDUKTOR

ABSTRAK

Pembungkusan mikroelektronik merupakan salah satu cabang kejuruteraan yang melibatkan kajian tentang pelbagai kaedah penyambungan komponen ke substratum di samping menjadi bahan penyambung. Teknologi pengikatan *die* yang menghubungkan die dan peranti ke seluruh sistem, memainkan peranan penting untuk memastikan keseluruhan sistem berfungsi secara konsisten. Teknologi serpihan flip (FC) telah diperkenalkan oleh IBM pada awal 1960-an untuk teknologi logik pepejal mereka. Teknik pengikatan *die* berbeza mengikut aplikasi peranti yang dibungkus. Parameter kefungsian yang kritikal untuk teknologi ikatan serpihan flip seperti pengikatan pelekat, pengikatan pateri aliran semula, pengikatan termosonik dan pengikatan pemampatan thermos adalah penting bagi industri pembuatan yang terlibat dalam pemasangan *backend.* Dalam kajian ini, satu tabulasi komprehensif bagi semua proses ikatan FC dibentuk. Dua pendekatan digunakan untuk mendapatkan maklumat ini.Pendekatan utama adalah untuk membuat eksperimen berasaskan simulasi untuk mengkaji tekanan maksima yang dialami oleh pakej semikonduktor semasa proses ikatan FC. Pendekatan tambahan yang lain ialah menggunakan kajian literatur sistematik (SLR), di mana semua parameter kefungsian yang kritikal (CTF) dikenalpasti, dinilai dan disintesis daripada sumber yang terdapat pada pemasangan *backend* dalam dunia proses semikonduktor. Dalam eksperimen simulasi ini, perisian sumber terbuka Elmer digunakan untuk setiap parameter berbeza dari jenis substratum, ketebalan die dan suhu proses.Keputusan simulasi menunjukkan tekanan tertinggi dialami oleh pakej FC yang mempunyai ketebalan *die* dan suhu proses yang lebih tinggi. Peningkatan dalam kekakuan *die* yang lebih tebal telah menguatkan ketegangan pada sambungan yang disebabkan oleh berbezaan pekali pengembangan haba (CTE). Begitu juga, tekanan meningkat pada suhu ikatan yang lebih tinggi akibat pengembangan yang berlaku dalam pakej semikonduktor. Di samping itu, sifat terma bahan bagi setiap jenis substratum juga menyumbang kepada tekanan maksimum keseluruhan pakej. Julat tekanan maksimum pakej bagi setiap kaedah ikatan FC: pematerian *reflow* dari 5.36E + 08 N / m^2 hingga 7.38E + 08 N / m^2; Pelekat dari 3.77E + 08 N / m^2 hingga 5.57E + 08 N / m^2; Thermosonik dari 2.21E + 08 N / m^2 hingga 9.48E + 08 N / m^2; TCB dari 4.77E + 08 N / m^2 hingga 1.09E + 09 N / m^2. Hasil yang diperolehi daripada SLR terbahagi kepada 1) teknologi proses FC, 2) geometri pakej, 3) parameter mesin, 4) kebolehpercayaan proses FC, 5) peralatan ikatan serta 6) cabaran dan masa depan. Secara keseluruhanya, komposisi bagi spektrum parameter CTF yang berlainan ini ditabulasi bersama untuk setiap proses ikatan FC. Penemuan dalam kerja penyelidikan ini akan memberikan pengetahuan yang komprehensif mengenai teknologi ikatan serpihan flip dan seterusnya memudahkan kerja penyelidikan di masa hadapan untuk meningkatkan kecekapan mana-mana teknik ikatan die.

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ABSTRACT

As a multidisciplinary branch of engineering, microelectronic packaging involves the study of various methods of joining components to substrate in addition to interconnecting materials. Die attach technology, which connects the die and device to the rest of the system, plays an important role to ensure the entire system works consistently. Flip chip (FC) technology was developed by IBM in early 1960s for their solid logic technology. Die bonding techniques vary according to the requirements of the application of the packaged devices. Critical to functional (CTF) parameters of FC die bonding technologies such as adhesive bonding, solder reflow bonding, thermosonic bonding and thermo-compression bonding are crucial for any manufacturing floor involved in this backend assembly. In this work a comprehensive tabulation of all these FC bonding process was formed. Two pronged approach was used to obtain this information. The main prong approach was to embark a simulation based experiment to study the semiconductor package stress during the FC bonding process. The other supplementary approach used a systematic literature review (SLR), where all the critical to functional (CTF) parameters were identified, appraised and synthesized from the available cornucopia of the backend assembly in the semiconductor process world. In the simulation experiment, open source software Elmer was utilized for each varied parameter from substrate type, die thickness and process temperature. The results of the simulation shows higher stress in FC package with thicker die and higher process temperature. Increase in stiffness of thicker die amplified the strain induced in interconnect caused by coefficient of thermal expansion (CTE) mismatch. Similarly the stress elevated at higher bonding temperature as a result of expansion that happened within the semiconductor package. In addition, material thermal properties of each substrate type also contributes to the overall maximum package stress. Range of maximum package stress for respective FC bonding method: Solder reflow from 5.36E+08 N/m^2 to 7.38E+08 N/m^2; Adhesive from 3.77E+08 N/m^2 to 5.57E+08 N/m^2; Thermosonic from 2.21E+08 N/m^2 to 9.48E+08 N/m^2; TCB from 4.77E+08 N/m^2 to 1.09E+09 N/m^2. The output from SLR were documented into 1) FC process technology, 2) package geometry, 3) machine parameter, 4) FC process reliability, 5) bonding equipment as well as 6) challenges and future. Finally, this compositions of varied spectrum of CTF parameters were tabulated together for each respective FC bonding process. The findings in this research work will provide a comprehensive knowledge of the flip chip die bonding technology and easier for future research work as to improve the efficiency of any of the die bonding techniques.

CHAPTER 1 : INTRODUCTION

1.1 Overview

As a multidisciplinary branch of engineering, microelectronic packaging involves the study of various methods of joining components to substrate in addition of providing physical protection, mechanical support and interconnect for semiconductor devices for them to function in a specific condition. Packaging technology advances along with the rapid development of transistor technology which continues to follow exponential progress by Moore's Law. Development of advance packaging technology is carried out while the semiconductor market continues to exert lower costs pressure. Die attach technology, which connect the die and device to the rest of the system, play an important role to ensure the entire system works consistently.

Wire bonding technology has been used for many years in order to form interconnection between integrated circuit (IC) and substrate. This technology was originated along with AT&T's beam lead bonding around 1950s. Bonding wires evolved from gold (Au) to copper (Cu) and most recently silver (Ag) wire has been reported. Nevertheless, Au wires are still widely used in lower pin count microelectronic packaging (Gan & Hashim, 2015). As the industry moves to low cost packaging, Cu slowly replaced Au wires although it faces more issues during temperature cycle (TC) and pressure cooker test (PCT). Palladium (Pd) coated Cu wires was introduced as to overcome this drawback (Breach, 2010).

Conversely, flip chip technology was developed by IBM in early 1960s for their solid logic technology. Three terminals transistor was the first IBM flip chip whereby Ni/Au plated Cu balls embedded in a Sn–Pb solder bump (Davis, Harding, Schwartz, & Corning, 1964). It was developed due to requirement of greater package density and higher performance device. The active IC will be facing downwards and the electrical terminals are usually made of solder or control collapse chip connection (C4) technology as to form connection between IC and substrate (Greig, 2010). Finer pitch applications foresee limitation and hence copper pillar technology was introduced. Flip chip process does involve flux application, placement and reflow as well as dispensing underfill material in order to restrain the large contraction/expansion between the die and substrate. Wire bonding on the other hand, could not match the density of flip chip although with finer pitch wires as the electrical connection covers the entire are of IC for the latter (Elenius & Levine, 2000).

The comparisons between these two technologies were shown in Table 1.1 and Figure 1.1. Hierarchically, semiconductor devices in a wafer level are being interconnected (0-level interconnection), and these devices then are connected externally to a substrate via first-level interconnection technology. Subsequently, a higher level of interconnection (board-level and system-level interconnection) needs to be established for the devices to be connected externally. There are various methods available in flip chip die attach, such as (i) adhesive bonding, (ii) thermosonic bonding ,(iii) solder reflow and (iv) thermo-compression bonding (TCB).

Table 1.1: Comparison between wire bonding and flip chip (Charles, 2009) ;(Qin, Yue, Zhang, & Yang, 2015); (Salam, Virseda, Da, Ekere, & Durairaj, 2004)

Wire bonding	**Flip Chip**
• Flexibility	• Device speed
• Infrastructure	• Power and ground distribution
• Cost	• I/O density with area array
• Reliability	• Package size/form factor
	• Lower resistance
	• Reliability

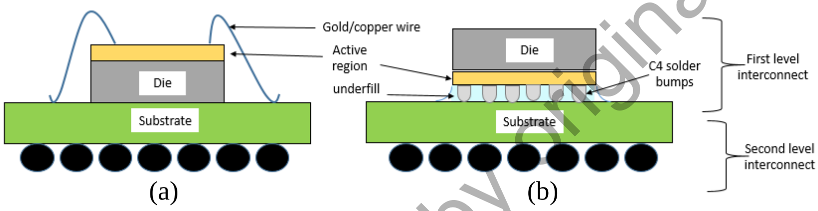

Figure 1.1: Illustration of a) wire bonding b) flip chip

Solder mass reflow technique have been used extensively for almost 50 years for the flip chip assembly. Tin lead solders are the primary materials used to form interconnections between the flip chip and substrate. The legislative ban on lead due to human health and environmental concerns came into full implementation in 2006 (Li, Lee, Evans, & Baldwin, 2011). Many types of lead free solders were introduced thereafter such as SnCu (El-Ashram & Shalaby, 2005), SnAg (J. Tsai, Hu, C. Tsai, & Kao, 2003) or SnAgCu (Chellvarajoo, Abdullah, & Khor, 2015) but none has identical physical and metallurgical properties similar to Pb. The SnAgCu solder can be regarded as the most promising candidate among all the proposed lead free solders. Thermal profiles – ramp to soak (RTS) or ramp soak spike (RSS) can be regarded as the most important factor in any reflow soldering process. The RSS thermal reflow profiles has four zones which are preheat, soak, reflow and cooling while RTS thermal profile does not have the soak zone (Salam et al., 2004).

Adhesive bonding is widely used in temperature sensitive components which includes image sensor, organic based transistor and liquid crystal display. This joining technique involves electrically conductive adhesives that bond by evaporation of a solvent or by curing a bonding agent with heat, pressure, or time. This promising technology offers following advantage comparing to solder: 1) lower assembly temperature which helps to reduce joint fatigue and stress cracking problem; 2) lower manufacturing costs by elimination of soldering and underfill process; 3) can be used in extreme fine pitch applications (Dudek, Berek, Fritsch, & Michel, 2000) and (Yin, Alam, Chan, Bailey, & Lu, 2003). The electrically conductive adhesives are available in the form of either paste or film. Isotropic conductive adhesive (ICA) and anisotropic conductive adhesive (ACA) are example of conductive adhesives available as paste. Conversely, anisotropic conductive film (ACF) is available in the form of film. The loading level of conductive fillers or percolation theory can also be used to clearly distinguish between ACA and ICA (Liong, Wong, & Burgoyne, 2005).

The application of thermosonic bonding was initially used in wire bonding method which was introduced by Alexander Coucoulas in 1960s. Over the years, this promising technology has been widely used in flip chip applications with low pin counts such as MEMS chips, LED packages, optoelectronic module and surface-acoustic-wave filter in telecommunication applications. The metallurgical joining of the thermosonic bonding is more reliable in reliability compared to solder interconnect and conductive adhesive (Tomioka, Iguchi, & Mori, 2004). Bonding process of thermosonic flip chip happens as the gold bumps are joined to the flexible or rigid substrate material using ultrasonic energy and heat under certain pressure (Tian et al., 2011).

Flip chip process which assembles the chip with Copper (Cu) pillar to the substrate using reflow oven do face multiple challenges such as die shift, high low-k stress, short connections due to bump bridging and die crack when the bump pitch lower than 100µm. All these drawbacks can be solved with TCB. It is another type of chip attach technology which is gaining quick popularity in the advanced semiconductor devices such as TSV-2.5D assembly and TSV-3D die stacking apart from the existing conventional chip on board flip chip assembly (Nonaka et al., 2014). Almost all the studies related to TCB uses pre-applied underfill such as NCP and NCF. The NCP is applied prior to bonding while NCF applied directly to the source wafer (Clauberg et al., 2014). Understanding the technology will be investigating the fundamentals of the technique which includes the mechanism, materials used, functional parameters, potential failure and other relevant elements.

1.2 Problem Statement

The flip chip bonding techniques available in the industry for semiconductor applications were introduced briefly in the previous section. As for the adhesive technique, Lin and Zhong (2008) evaluated the key factors that effects the adhesives joining specifically on ACA while recent advances in electrically conductive adhesives were reported by Lu and Wong (2013). A research on the adhesive flip chip bonding using ACF and NCA were reported by S. Kim and Y. Kim (2013) covered the principles, applications, key process parameters as well as works done in order to improve the device reliability. Nevertheless, ICA and ACA technology which is also electrically conductive adhesives were not included. The curing time which also plays vital role in the overall joint quality should be part of the work similar to the equipment that is currently available in the market to support this bonding technique. As for the TCB technique, Eitan and Hung (2015) identified the key challenges, key bonding process and equipment used in Intel for high volume manufacturing (HVM). In contrast, comprehensive study on the remaining two flip chip bonding techniques which are covered in this thesis namely thermosonic and solder reflow were very minimal to the best of author's knowledge search.

However there are couple of works that synthesized the overall evolutions that foreseen in flip chip technology. Recent advances and newer trends in flip chip technology was reported by Lau (2016) and Perfecto and Srivastava (2013). The author's scope of study included package substrate, wafer bumping, assembly and underfill for flip chip technology. Similar work were reported by Kang, Shih and Bernier (2013) but their scope of study focused more on the different types of interconnects in flip chip – lead solder bumps, lead free solders, copper pillar and gold stud bumps. They also covered common reliability issues that associates with the use of lead free solders.

The study completed by Lee, Wang and Kim (2016) appraised six major bonding techniques available in microelectronic packaging such as adhesive, lead free soldering, silver-indium bonding, solid state bonding, silver flip chip and 10um silver flip chip with solid state bonding. Scope of study was not standardized among each of the technique and table of summary was not presented as a final comparison among all the reviewed techniques. For example, the reliability performance was only reviewed in silver-indium bonding technique and left out in other bonding techniques.

Upon exhaustive search, there was minimal information on package stress during FC bonding process. This is critical information needed to appraise and choose from the available FC bonding techniques. The other aspects where the need for CTF information is found to be sporadically all over the literature database. Thus, it can be summarized that minimum work or none were done in analysing all four FC bonding technique (solder reflow, adhesive, thermosonic, TCB) for obtaining the package stress during the process. Topping to this, there is also lack of comprehensive tabulation of CTF parameters of FC bonding process. The comprehensive CTFs' underlined here which are FC process technology, package geometry, machine parameter, reliability, bonding equipment as well as challenges and future will be covered in this paper.

1.3 Objectives

The main objective would be to complete a comprehensive tabulation on CTF parameters of available flip chip die bonding technology in semiconductor industrial which could be used as a quick reference during process development of next generation FC die bonding technology. For each FC bonding technologies reviewed accordingly, the sub objectives would be:

i. To study and analyse on the maximum package thermal stress experienced by the semiconductor package during die bonding process for each flip chip die bonding technique using a computer-aided engineering software, Elmer.
ii. To identify the evolution of process method as well as the interaction of overall package and interconnect geometry that directly influences the overall joint quality.
iii. To synthesize machine parameters that impacts overall joint quality and available bonding equipment including material and process capabilities.

iv. To evaluate the reliability tests, key failures and continuous reliability enhancement as well as to identify the key challenges that limits the applications on next generation technology.

1.4 Scope of Study

In this dissertation, simulation study carried out in order to understand the maximum thermal stress experienced by the package during die bonding process for each flip chip die bonding method. Extracting the other CTF parameters were approached using systematic literature review. The scope dwelled here for FC bonding includes solder reflow, adhesive, thermosonic and TCB technique. Understanding this in depth would provide a better window of understanding for the industrial applications, whereby a tabulated reference would be resourceful in process development during engagement of die bonding.

1.5 Report Layout

This study consisted of six chapters and a short summary of each chapter is discussed briefly in this section.

Chapter 1 concisely introduced the advancement in semiconductor packaging which included the comparisons of wire bonding and flip chip die attach technique. Problem statement subtopic provided context for the research study and generated the questions which the research aimed to answer. Finally, the objectives and scope of study concluded this chapter.

Chapter 2 focused on systematic literature review approach to identify, appraise and synthesize all the CTF parameters from a cornucopia of available FC semiconductor process. Major findings are also concluded at the end of the chapter.

Chapter 3 discussed on the methodology used to carry out both customized simulation experiment and systematic literature review as to achieve all the objectives of the study.

Chapter 4 presented the vital findings from the simulation experiment in a comprehensive manner and the projected first objective to be reviewed to ensure the goals set are still in contact.

Chapter 5 concluded the whole thesis by summarizing the research done and proposing future works to the study conducted.

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CHAPTER 2 : SYSTEMATIC LITERATURE REVIEW

2.1 Introduction

Systematic literature review can be regarded as a piece of research by its own nature which addresses broader problem statements than single empirical studies ever can. This kind of review able to solve problems by identifying, critically evaluating and also integrating all the important findings from multiple individual research works. In this chapter, the scope of systematic literature review and CTF data extraction to meet three out of four objectives specified in Chapter 1 revolved around FC die bonding technologies which are solder reflow bonding, adhesive bonding, thermosonic bonding and thermo-compression bonding (TCB). It has been divided into six CTFs as shown in Figure 2.1.

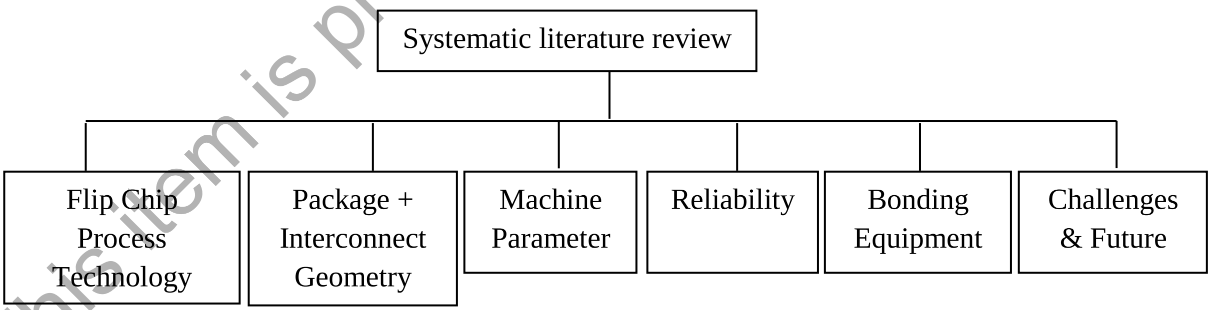

Figure 2.1: List of sub-topics covered as part of systematic literature review

The scope of study covered in each of the sub topic are briefly listed as below:

I. Flip chip process technology: Summary of process technology and bonding sequence differences that lies within each of the bonding technique.

II. Package geometry: Influence of die and substrate geometry on overall bonding quality.

III. Machine parameter: List of parameter that plays vital role in order to achieve reliable interconnect between die and substrate in every bonding process.

IV. Reliability: Types of reliability tests carried out in each bonding method as to evaluate the overall joint reliability with respect to differences in machine parameter and incoming materials.

V. Bonding equipment: Example of available bonding tools which can be used to perform bonding in respective bonding technique.

VI. Challenges and future: Key aspects in each bonding method that need to be addressed as to expand the overall application along with semiconductor packaging technology evolution.

All the CTF's will be identified, appraised and synthesized from a cornucopia of available back end assembly process. The cornucopia consist of:

a) Academic scientific publications

b) Industrial research white papers

c) Machine datasheets

d) Patents

e) Engineering technical paper

f) Reliability test standards and regulations

Dramatic increase in amount of research works done over the past few years had made impossible for professionals to keep up to date with all the key findings. Systematic review allows concise synthesis of a large body of research given the amount and complexity of available information and limitations of time. Many universities around the world encourages students to perform systematic reviews as part of their postgraduate study. The students were exposed to different type of research methodology which helped the students to develop skills in identifying, appraising and synthesising research findings. Table 2.1 briefly summarizes the key differences between traditional and systematic literature review.

Table 2.1: Comparison between traditional and systematic literature review (Siddaway, 2014; Boland, Cherry & Dickson, 2017)

	Traditional Literature review	**Systematic literature review**
The review question/topic	Topics are broad in scope and the goal of review is to gather information that supports particular viewpoint.	Begins with well-established problem statement to be answered by the review. Reviews are carried out in an unbiased, transparent and reproducible way with the aim of finding all existing research works.
Searching for studies	Searches are not exhaustive or fully comprehended.	Attempts are made to find all existing published and unpublished literatures on the research question. The process is well documented and reported.
Study selection	Often lack clear reasons for why studies were included or excluded from the review.	Reasons for including or excluding studies are explicit and informed by research question.

2.2 Flip Chip Process Technology

This sub topic provides a glimpse process introduction of each flip chip bonding techniques which were mentioned in the scope of the study. Flow charts and illustrations were used to summarize the bonding sequence as well as the key process differences.

2.2.1 Solder Reflow Flip Chip

Soldering is a process of joining two pieces of metals using a filler metal, known as solder which has a low melting point (below the melting point of the work piece). Since the joints are formed using reflow method, an optimized temperature profile is necessary. In general there are 3 types of heat transfer in reflow technique; which are conduction, convection and infrared (Hwang, 2012). As for the flip chip devices, convection and conduction are the most commonly used heat transfer mechanism in the reflow soldering. Both can be classified as contact methods in which the mass air flow are provided by a combination of a fan and an electric resistor heating element. Temperature difference need to occur in order to transfer effectively the heat. In addition, the heat transfer rate is directly proportional to the temperature difference. Parameters in reflow profile do have direct influence on the reliability of solder joint as it influence the formation of intermetallic layers within the solder joint. Flux is widely used in flip chip technology as to remove the oxides/contaminations from the bump surfaces during reflow process. Commonly used method to apply flux on either the die solder bump or Cu pad on substrate are flux dipping and flux dispensing respectively.

2.2.1.1 Flip Chip Reflow Thermal Profile

Thermal profile can be regarded as the most important factor in any reflow soldering process. The overall quality of solder joint is directly dependent on the thermal profile. The main aim of reflow process is to form quality joint without damaging or overheating the printed circuit board (PCB). Numerous publications have focused on the impact of thermal profile on the reliability of solder joint. Salam et al. (2004) conducted study on the effect of two extensively used reflow profile; RTS and RSS on the IMC layer thickness and microstructure of Sn-Ag-Cu solder. The RSS profile is used for no clean chemistries and it is not recommended for water soluble chemistries. This is because the soak zones which available in RSS profile are believed to separate the activators of the solder paste prematurely and provide lesser wetting. Boards that have multiple components benefited well from the RSS profile. Figure 2.2 exhibits the example of RTS and RSS thermal profile.

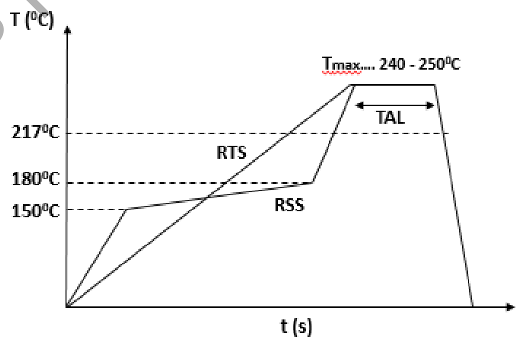

Figure 2.2: Example of RTS and RSS thermal profile

The RTS profile has multiple advantages compared to the RSS profile such as below (Mir & Kumar, 2008):

a) Shiner and brighter solder joints since flux vehicle still exist during the pre-heat stage

b) Promote better solder wetting

c) Easy to control the ramp rate, hence less defect to solder and lower thermal shock

The RSS thermal reflow profiles has four zones which are preheat, soak, reflow and cooling while RTS thermal profile does not have the soak zone (Salam et al., 2004)

I) Pre-heat zone: In this zone, the temperature are ramped up at a rate of 10 °C to 30 °C. The solvent in the paste/flux begins to evaporate in this zone.

II) Soak Zone: This zone is only available in the RSS thermal profile. The main reason for having the soak zone is to ensure an equilibrium temperature achieved among all the components before it reaches the reflow temperature of solder. The zone helps to eliminate solder defects such as solder balling, non-wetting, voids and charred residues. Flux is also activated at this zone in which the oxidations on the solder pads can be effectively removed and thus prepare surface for solder wetting on next stage. The soak time indicates the total time the component goes through soak zone.

III) Reflow zone: The flux reduces surface tension at the juncture of the metals to accomplish metallurgical bonding, allowing the individual solder to combine in this zone. The maximum reflow temperature (peak temperature) is achieved in this zone during the time above liquid (TAL). The TAL is often referred as the total time when the solder is heated up to a temperature above the solder melting temperature. The peak temperature of the lead free solder is between 2400 °C to 2500°C.

IV) Cooling zone: In this zone, the temperature gradually reduced and the solder joint solidification process takes place.

2.2.1.2 Application of Flux in Solder Reflow Flip Chip

The flux is widely used in flip chip technology as to remove the oxides/contaminations from the bump surfaces during reflow process. Moreover, flux also promotes wetting of solder balls and copper surfaces on conductive pads. The tackiness of flux helps to hold and maintain the flipped chip in position during die placement and reflow process. Commonly used method to apply flux on either the die solder bump or Cu pad on substrate are flux dipping and flux dispensing respectively. In general, there are two types of flux which are used commonly in semiconductor; water soluble and no-clean flux. The difference lies on clean flux type which requires additional process as to clean the flux after reflow process.

In flux dipping method, the flip chip with the solder bumps facing downwards is dipped into a very thin layer of flux. Utilizing this method helps the flux to concentrate in really needed places. However, solder bump height variation could pose drawback as to achieve the desired flux depth which is 50 % of the ball diameter. Flux dipping method works well with high viscosity fluxes and not with fluxes with high evaporation rate (Jacobson & Humpston, 2004). Key differences between both methods are summarized in Table 2.2.

Table 2.2: Key differences between flux dipping and flux dispensing (Jacobson & Humpston, 2004; Master et al., 2000 ;Wei, Li, & Lei, 2014)

Criteria	Flux Dipping	Flux Dispensing
Type of flux	High viscosity	Low & High viscosity
Flux Coverage	Moderate	Better
Flux exposure to air	Always	After spray
Flux clean interval	Every 4 hours	Every 1 week

Placement alignment inspection before the flux dipping could create negative impact to the placement accuracy due to mechanical contact of flip chip with the flux carrier. Nevertheless, inspecting the bump surfaces with the presence of flux also possess some risks. Asymmetric bump pattern recognition is used in order to avoid placing the die in wrong orientation. The amount of flux dipped for each die need to be precisely controlled. The flux surface needs to be smooth enough and the liquid level remains unchanged after multiple dipping sequence. Flux on the conventional dipping process using rotary tray is placed on plate large area. Hence the flux solute content increases as it is exposed to the air.

In order to overcome all these issue, Wei et al. (2014) proposed gluing method for flux dipping. In this method, the flux will be eventually placed in a sealed container and subsequently the flux will be transferred to the flux groove. The chip brought into the flux groove and gets dipped with just enough flux. The container moves through the groove for every single die as to flow flux into the groove and also to remove any excess flux. By doing this, the flux solvent will not be evaporated as the exposed area of flux is reduced. Dropping of liquid level after multiple dipping count can be avoided too.

The process flow for flux dipping are explained as below and shown in Figure 2.3.

a) Firstly, the creamy flux applied to rotating disk at dipping station.

b) Secondly, bonding placement head picks the die, aligns the flip chip on top of disk at dipping station and finally dips the flip chip into the flux.

c) Next, the flip chip lifted from the dipping station while the doctor blade resumes spinning.

d) After that, the chip is brought to the board and placement alignment done using optical camera.

e) Finally, the flip chip is placed on the substrate pad and reflowed in an oven.

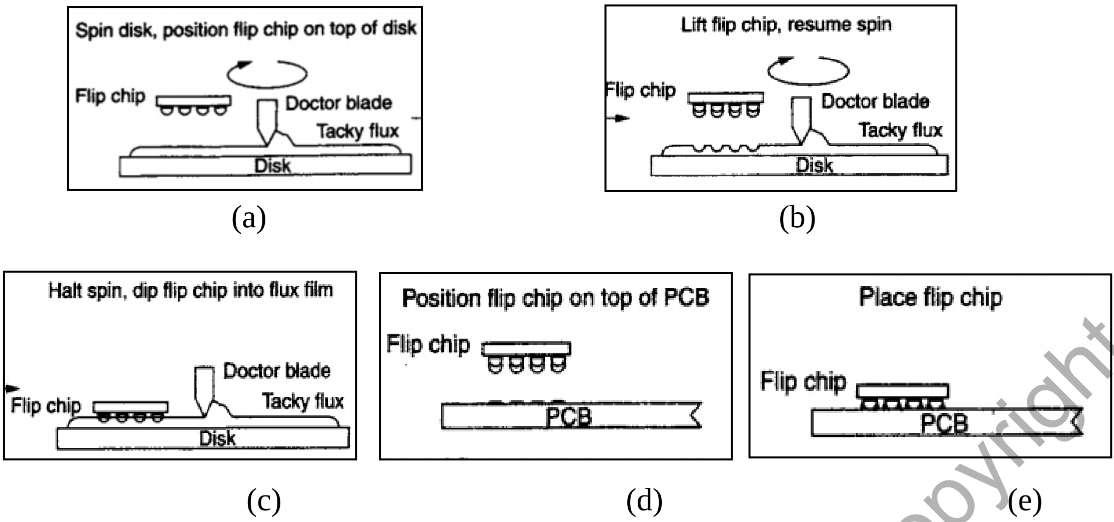

Figure 2.3: Dip Flux process flow (Wei et al., 2014)

Chances of flux climbing over the die edge is very high in flux dipping method due to the usage of high viscous flux. This eventually contaminates the die surface as a result of too much flux. Dispensing flux using the jetting technology replaces the traditional method as it provides better control on the flux amount as well as the location of fluxing. A uniform amount of flux can be applied to the substrate by utilizing the spraying technique. Moreover, many types of pattern and geometries of flux can be done while maintaining good edge definition (0.5 mm to 1.0 mm).

Higher throughput can be achieved compared to flux dipping method as the flux dispensing process step is done in separate tool. Dot jetting is widely used compared to line jetting. Both methods do use the coaxial air supply as to spread evenly the flux on the substrate. The flux is dispensed in a circular pattern (dot) in an array which forms a pattern on the substrate as for the dot jetting. The line jetting is utilized for applications that requires the flux to be dispensed quickly and thin layer (Master et al., 2000; Lee, Lin, Chang, Jiang, & Chen, 2009). The process flow for flux dispensing are explained as below:

a) First, the flux dispensed on the substrate covering the C4 areas.

b) The tray/carrier travels to the bonding tool.

c) Next, placement head picks the die and align using optical camera.

d) The die placed on the substrate and finally reflowed in oven.

In general, water soluble fluxes can be categorized into organic and inorganic based on their compositions (Shangguan, 2005). The organic fluxes are the most active available flux and it contains high amount of ionic substances which could cause serious corrosion to the electronic component. Hence cleaning process needed in order to remove all the by-products after thermal reflow process. Cleaning is done in three stages; washing, rinsing and drying. In the washing stage, the flip chip package will be sprayed with high pressurized de-ionized water at certain angle in order to remove the organic flux residue. Next it is rinsed with warm to hot water in order to remove any leftover by-products. Finally the flip chip package will be dried at the drying stage using hot air and heat. Typical wash temperature is around 55 °C while the rinse temperature varies from 30 °C to 80 °C. Organic acids, amines and halides with salts are the activators for this type of flux. While as for the flux vehicle, polyglycols, polyglycol surfactants and glycerin are used.

Flux removing process after solder reflow is eliminated by using the no-clean flux (Jacobson & Humpston, 2004). This eventually reduces the manufacturing costs and increases the cycle time of the products. Typically no clean flux lefts some residues but it would not have any negative impact on the assemblies. Newer generation of no clean fluxes are water based and does not have volatile organic compounds (including alcohol). A wide range of chemical ingredients are used to formulate flux which contains high alcohol solvent with small amount of active ingredients.

Normally the activators in the flux is weakened to lower levels in order to eliminate the cleaning step. It contains low content of halides compared to traditional clean flux; 2 to 3wt% vs 25 to 35wt% (Lee et al., 2009). However there is another method whereby activators having normal strength mixes with gelatine and undergoes polymerization at the soldering temperature. In general, sufficient flux need to be applied to order to achieve good solder ability. Furthermore, uniform heat should be given in order for the flux to fully react and leave harmless by-products.

Three surface energies dominates the wetting reaction during wetting balance tests as shown in Figure 2.4; surface energy of the substrate to the flux, surface energy of the liquid solder to flux and surface energy of the substrate to liquid solder. Displacement of solder due to upward force which caused by partially immersed substrate takes place at the initial stage of wetting balance tests. Hence non-wetting happens as the liquid solder on substrate transforms to concave shape. Next, when the neural condition of wetting happens, the liquid solder becomes flat and wetting takes place. Lastly, the surface tension between substrate and flux will cause the liquid solder to climb along the substrate. Meniscus height represents the rising height above the liquid solder surface.

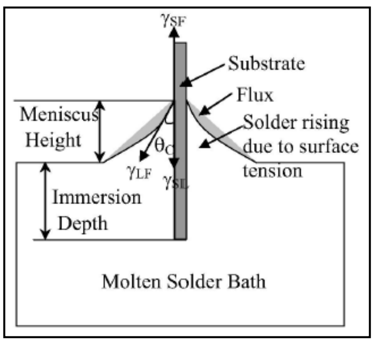

Figure 2.4: Schematic diagram of wetting balance test
(Rizvi, Bailey, Chan, & Lu, 2006)

Addition of small amount of Ni in the Sn-0.7Cu solder helped the flux spread well over the soldering surfaces and exhibit better wetting behaviour as deduced by Rizvi et al. (2006). In their study three types of commercially available fluxes (no clean, non-activated and water soluble) along with two different lead free solders (Sn-0.7Cu and Sn-0.7Cu-0.3Ni) used on the Cu and Ni substrate. The non-clean flux showed better wettability performance for Cu substrates as it has the lowest solder-flux interfacial tension value (370mN/mm).

Conversely, the water soluble flux have better wetting capability on Ni substrates although it has higher solder-flux interfacial tension value (445 mN/mm). By nature, the water soluble flux contains reactive compound that cleans the soldering surface and also wetting component that helps to spread the flux. The non-activated flux has highest solder-flux interfacial tension as well as poor cleaning capability which made it to be unsuitable for both Cu and Ni substrates. It was also found that the contact angle is inversely proportional to the wetting force and meniscus height. Gu et al. (2015) investigated the effect of adding nanoparticles of iron oxide, Fe2O3 on the wettability of SAC solder which has lower Ag content. Commonly used SAC solders does have Ag content of more than 3% and hence better wettability and thermal mechanical fatigue properties achieved. However the study proved that good wettability can be attained with Ag content of 1 % (SAC105) with the addition of 0.4wt% nanoparticles of iron oxide. Higher content of Ag in solder do have negative effect such as high costs and large brittle Ag3Sn.

Whereas, the iron oxide chosen due to excellent magnetic and electrical properties, availability and lower cost. As shown in Figure 2.5, 0.4wt% weight yields the lowest wetting time (1.10s) along with highest wetting force (3.35 mN). Theoretically, lower wetting time and higher wetting force indicates better wettability of a solder.

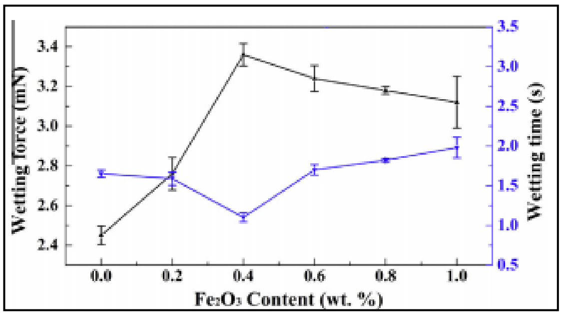

Figure 2.5: Mean maximum wetting force and mean wetting time of SAC107 at different Fe_2O_3 content (Rizvi et al., 2006)

2.2.1.3 Solder Reflow Flip Chip Bonding Process

The typical bonding procedure for flip chip solder reflow is summarized in the flow chart in Figure 2.6.

Flux is applied on the substrate C4 bump area using flux dispense tool (dipping or spraying)

↓

Substrate is transferred to the flip chip die placement tool

↓

The bonding head picks the die from the tape & reel. Optical camera is used to inspect/align the die/substrate bump

↓

The bond head places die on the substrates. Next, it will go through placement accuracy check

↓

The assembly will go through reflow oven in order to melt the solder and form reliable interconnect

↓

Inspection for total bump misalignment and die crack

Figure 2.6: Flip chip solder reflow sequence

2.2.2 Adhesive Flip Chip

Adhesive flip chip bonding technology normally applied to temperature sensitive components or flexible electronic appliances such as image sensor, organic based transistor and liquid crystal display. This promising technology offers the following advantage comparing to solder: 1) lower assembly temperature which helps to reduce joint fatigue and stress cracking problems; 2) lower manufacturing costs by elimination of soldering and underfill process; 3) can be used in extreme fine pitch applications. The electrically conductive adhesives are available in the form of either paste or film. Isotropic conductive adhesive (ICA) and anisotropic conductive adhesive (ACA) are the two example of conductive adhesives available as paste. Conversely, anisotropic conductive film (ACF) is available in the form of film. Figure 2.7 illustrates the difference between ACA and ICA. The percolation theory as shown in Figure 2.8 explained clearly the difference between ACA and ICA by taking into account the loading level of conductive fillers.

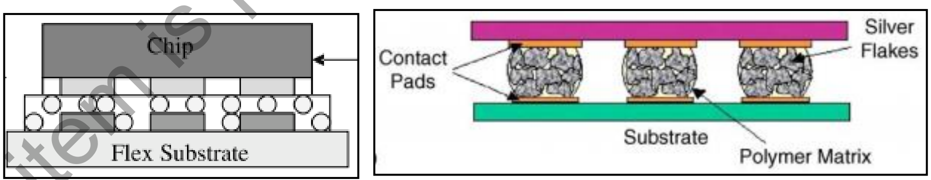

Figure 2.7: Schematic illustration of a) ACA and b) ICA (Li & Wong, 2006)

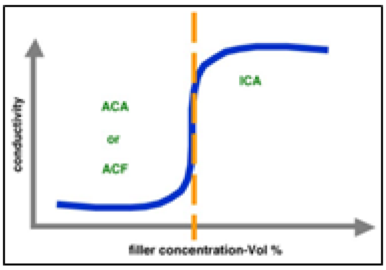

Figure 2.8: Conductive fillers volume difference between ACA and ICA
(Liong, Wong, & Burgoyne, 2005)

2.2.2.1 Anisotropic Conductive Adhesives (ACAs) bonding

The ACA bonding technology has been investigated as a substitution to lead free solder in fine pitch and high temperature sensitive components. These adhesives are made of conductive particles and non-conductive polymer matrix. The main objective of these adhesives is to hold at least one conductive particle between the flip chip and corresponding substrate. Furthermore, the adhesive can be deposited onto the overall contact region due to its anisotropic property which eventually increases the mechanical reliability (Yim, Hwang, & Phaik, 2007); (Li & Wong, 2006). Unlike ICA, this promising technology can be used in very fine pitch applications without creating any short circuit between the adjacent bumps. The lesser quantity of conductive particles due to lower percentage (1-5 %) of metal fillers helped to create reliable electrical conductivity only in the Z-direction while maintaining insulation in the x and y planes (Li & Wong, 2006).

ACA is available in two distinct forms which are paste (ACP) and film (ACF). The ACPs can be printed using screen and stencil or dispensed with a syringe while the ACFs are normally deposited onto the substrate using pre-lamination technique. Additional manufacturing costs is required in order to cast a film and cut according to the chip size. This has made the ACP technology widely preferred in low cost flip chip assembly over the ACF. However there are some drawbacks such as tough storage requirement, shorter pot life and also difficulties to obtain consistent conductive particle distribution. Nevertheless, the ACFs worked well with the available technology in flat panel display module packages. The typical bonding procedure of flip chip with ACA is shown in the flow chart in Figure 2.9.