JUNCTIONLESS TRANSISTORS: PARAMETRIC STUDY WITH CONVENTIONAL DOPING IN MOSFETS

By

NURUL HUDA BINTI ABDUL RAHMAN
(1531711669)

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INSTITUTE OF NANO ELECTRONIC ENGINEERING
UNIVERSITI MALAYSIA PERLIS

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LIST OF ABBREVIATIONS

SCE	Short-channel effect
TCAD	Technology computer aided design
2D	2-Dimensional
3D	3-Dimensional
SOI	Silicon-on-insulator
JT	Junction transistor
JLT	Junctionless transistor
RF	Radio frequency
MOSFET	Metal oxide semiconductor field effect transistor
FinFET	Fin-field effect transistor
EOT	Equivalent oxide thickness
UTB	Ultra-thin body
BJT	Bipolar junction transistor
FET	Field effect transistor
IC	Integrated circuits
nMOS	n-type metal oxide semiconductor
S/D	Source/Drain
SS	Subthreshold slope
DIBL	Drain induced barrier lowering
AR	Aspect ratio
JNT	Junctionless nanowire transistor
IM	Inversion-mode
SNW	Silicon nanowire

JLSNW	Junctionless silicon nanowire
DC	Digital characteristics
AC	Analogue characteristics
CC	Constant current

LIST OF SYMBOLS

L_G	Gate length
T_{OX}	Gate oxide thickness
T_{BOX}	Buried oxide thickness
T_{Si}	Silicon body thickness
W_{Si}	Silicon body width
N_D	Donor dopant concentration
V_{TH}	Threshold voltage
V_G	Gate voltage
V_D	Drain voltage
I_{ON}	On-current
I_{OFF}	Off-current
I_{Doff}	Off drain current
g_m	Transconductance
g_d	Output conductance
C_{gg}	Gate-to-gate capacitance
f_{max}	Maximum oscillation frequency
G_{dsi}	Intrinsic source-drain conductance
C_{gs}	Gate-to-source capacitance
A_v	Intrinsic gain
f_T	Current gain cut-off frequency

Junctionless Transistor: Kajian Parametrik dengan Pemendapan Konvensional dalam MOSFET

ABSTRAK

Kemajuan teknologi hari ini telah dibangunkan secara pesat untuk menampung keperluan teknologi semasa yang menjadi sangat kompetitif dan permintaan yang tinggi untuk menampung gaya hidup manusia. Alat elektronik memacu pasaran dengan menyediakan cip pada kelajuan yang tinggi dan penambahan fungsi yang lebih baik. Hal ini telah menjadi semakin mencabar apabila ketumpatan dan prestasi transistor meningkat secara agresif. Pengecilan yang berterusan terhadap transistor konvensional akan memberi kesan teruk pada kesan saluran pendek (SCE), dan salah satu penyelesaian adalah simpang ultra-cetek. Persimpangan ultra-cetek adalah sangat mencabar kerana ia meningkatkan kos fabrikasi dan menyukarkan proses fabrikasi. Dalam kajian ini, transistor mempunyai jenis pendap yang sama pada saluran, penguras, dan sumber di mana simpang ultra-cetek telah dihapuskan. Oleh itu, ia dipanggil *junctionless transistor (JLT)*. Penyerapan tidak akan berlaku pada transistor di mana ia akan mengurangkan kos untuk teknik ultralaju penyembuhan pemanasan. Selain itu, ia membolehkan transistor yang dapat direka dengan saluran yang lebih pendek jika tiada kecerunan kepekatan doping di antara penguras dan saluran atau sumber dan saluran. Prinsip operasi *junctionless transistor* dikaji dengan melalui simulasi berangka yang menggunakan alat simulasi TCAD. Pertama, prestasi peranti daripada 3 Dimensi (3D) silikon dalam penebat (SOI) *junctionless transistor* dengan 100 dan 10 nm panjang gerbang, telah dibandingkan dengan 3D SOI transistor konvensional (JT) dengan panjang gerbang yang sama. Dalam usaha untuk mencapai pengurangan penuh, parameter seperti fungsi kerja gerbang logam, kepekatan doping, dan dimensi telah dipertimbangkan secara khusus dalam proses simulasi. Merit-angka untuk ciri-ciri digital seperti voltan ambang (V_{TH}), arus semasa (I_{ON}), dan cerun *subthreshold* adalah parameter utama yang telah dikaji. Seterusnya, pencirian merit-angka terhadap analog dan frekuensi radio (RF) telah dilaksanakan. Berdasarkan kepada simulasi, 1) peranti JLT yang direka adalah lebih sesuai dengan fungsi kerja gerbang logam yang lebih tinggi daripada 5.0 eV manakala peranti JT yang direka adalah lebih sesuai dengan fungsi kerja gerbang logam pertengahan seperti 4.6 eV. 2) transistor JLT memerlukan fungsi kerja gerbang logam yang tinggi untuk mengawal saluran. 3) peranti JT adalah kurang sensitif terhadap perubahan kepekatan pemendapan, ketebalan badan silicon (T_{Si}) dan lebar (W_{Si}) berbanding dengan peranti JLT. Akhir sekali, prestasi peranti pada merit-angka analog dan RF menunjukkan bahawa, tidak ada perbezaan yang ketara di antara peranti JLT dan JT dengan kes kedua menunjukkan prestasi lebih baik sedikit, yang berkaitan dengan kapasitan gerbang-ke-gerbang (C_{gg}) yang rendah.

Junctionless Transistors: Parametric Study with Conventional Doping in MOSFETs

ABSTRACT

The advancement of today technologies has been aggressively developed as the needs of current technology that becoming competitive and demanding to accommodate human lifestyle. The electronic gadgets drive the market with the requirements to provide efficient chip functionality at higher speed and extra functionality. This has become more challenging as the transistor density and performance are aggressively increasing. Thus, continuous downscaling of the conventional transistor will lead to severe short-channel effect (SCE), and one of the solutions is a ultra-shallow junction. Ultra-shallow junction is very challenging as it increases in fabrication cost and difficulty in the fabrication process. In this study, the channel, drain, and source have the same type of doping where the ultra-shallow junction has been eliminated. Hence, it is called junctionless. There will be no diffusion will take place where it will remove the high cost for ultrafast annealing techniques. Besides that, it allows the transistor to be fabricated with a shorter channel if the gradient of the doping concentration is zero between drain and channel or source and channel. This operation principle of the junctionless transistor is investigated through numerical simulations using technology computer aided design (TCAD) simulation tools. Firstly, the device performance of 3-Dimensional (3D) silicon-on-insulator (SOI) junctionless transistor (JLT) with 100 and 10 nm gate lengths, have been compared to the 3D SOI junction transistor (JT) with the same gate length. In order to achieve full depletion, the parameters such as metal gate workfunction, doping concentration, drain bias, and dimension are considered in the simulation process. The digital figure-of-merits characteristics such as threshold voltage (V_{TH}), on-current, subthreshold slope, and drain-induced-barrier-lowering are the main parameters that have been investigated. Following next is the characterization on the analog and radio frequency (RF) figures-of-merit. Based on the simulations, 1) the designated JLT device is more suitable to the higher gate workfunction of more than 5.0 eV whereas the designated JT device is more suitable with mid-gap values of gate workfunction of 4.6 eV. 2) the JLT transistor requires high gate work-function to have control over the channel. 3) the JT device is less sensitive to the variation of silicon body thickness (T_{Si}) and width (W_{Si}) compared to JLT. Lastly, the device performance on analog and RF figures of merit shows that no significant different between JLT and JT with the latter case shows slightly better performance, related to lower gate-to-gate capacitance (C_{gg}).

CHAPTER 1

BACKGROUND

1.1 Introduction

Human lifestyle has been improving day by day with the help of newer technology as the needs of nowadays technology have been competitive and demanding. Then, the requirements to provide efficient chip functionality at higher speed have become more challenging as the transistor density and performance are aggressively increasing. Metal oxide semiconductor field effect transistor (MOSFET) is the most common transistor that has been used in both digital and analogue circuits. Single silicon microchip has been made up with few hundreds of transistors and it has gone up to over several billion today. This has been supported by Moore's law, where the number of transistors doubled every 12 to 18 months while price keeping unchanged. As a result, the size of the transistor has been miniaturized to support the industrial needs and it is become challenging to create high quality junctions.

Besides that, the miniaturized of the transistor will lead to higher leakage current where it will degrade the transistor performance. Many researches have been done to overcome these leakage current issues as it becomes a big obstacle to the transistor downsizing. The multi-gate structure such as Fin Field Effect Transistor (FinFET) (Lakshmi & Srinivasan, 2012; Makovejev et al., 2012; Nawaz, Dutta, Chattopadhyay, & Mallik, 2014; Seo, Yuan, & Kang, 2013), Si-nanowire (Bishnoi & Ghosh, n.d.; J. P. Colinge et al., 2011; Jean-Pierre Colinge et al., 2010; FERAIN, 2013; Larki, Hutagalung, Dehzangi, Saion, & Abedini, 2012; Mariniello & Pavanello, 2014; C. Park et al., 2012; Souza et al., 2011; Trevisoli, Doria, de Souza, & Pavanello, 2013), double-gate (Ávila-

Herrera et al., 2015; Dou, Wan, Jiang, Zhu, & Zhang, n.d.; Medhi, 2014; Rahul, Yadav, & Bohat, 2014; Wu, Jin, Chuai, Liu, & Lee, 2013; Wu, Jin, Kwon, et al., 2013), and tri-gate (D. Jeon et al., 2013; D.-Y. Jeon et al., 2013; Leuven, Ingenieurswetenschappen, & Elektrotechniek, 2008; S. J. Park et al., 2013; Paz & Pavanello, n.d.; Razavi, 2013; Rios et al., 2011) MOSFETs has been investigated by the researchers to overcome the leakage current issues. In addition, the application of high-k/metal gate (Ana, 2011; "Chapter 5 Effect of Gate Electrode Work Function Variation on Dc and Ac Parameters in," 2002; Gundapaneni, Ganguly, & Kottantharayil, 2011b; Lakshmi & Srinivasan, 2012; Leuven et al., 2008; Rahul et al., 2014; Wang, Shan, Dou, Wang, & Cao, 2015) technologies has been implemented down to 1.2 nm (Iwai, 2015) but the researches are continue. The manufacturing of equivalent oxide thickness (EOT) scaling down to 0.9 nm (Iwai, 2015) has shown that the continuous study on transistor has been done to overcome this challenge.

1.2 Research Background

1.2.1 Rational

Commonly, the existing planar or multi-gate transistor devices are based on the presence of junction which consists of drain, channel, and source as shown in Fig. 1.1 (a) to allow the current flow through or stop depending on the applied voltage. The junction is formed when there are two (2) semiconductor interfaces with different polarities between one another. The junction transistor is implemented not only for previous technology but also for advanced devices technology such as ultra-thin body (UTB/UTBB) (M K Arshad et al., 2013; Mohd Khairuddin Arshad et al., 2012; Litty, Ortolland, Golanski, & Cristoloveanu, 2015; Md Arshad, Othman, & Hashim, 2015) or FinFET architecture (Lakshmi & Srinivasan, 2012; Makovejev et al., 2012; Nawaz et al.,

2014; Seo et al., 2013). In those technologies, ultra-sharp doping junction gradients are needed to achieve better performance in an advanced scaled transistor. Thus, a high cost budget is required to manufacture the transistor because it has requires the development of high cost millisecond annealing techniques. Recently, there is a research that looking for a transistor that does not requires the present of junction i.e. the drain, channel, and source has same doping concentration as illustrate in Fig. 1.1 (b). This transistor is known as the junctionless transistor. Therefore, the continuous study on junctionless transistor has been done by most of the device researcher to overcome this challenge since 2010.

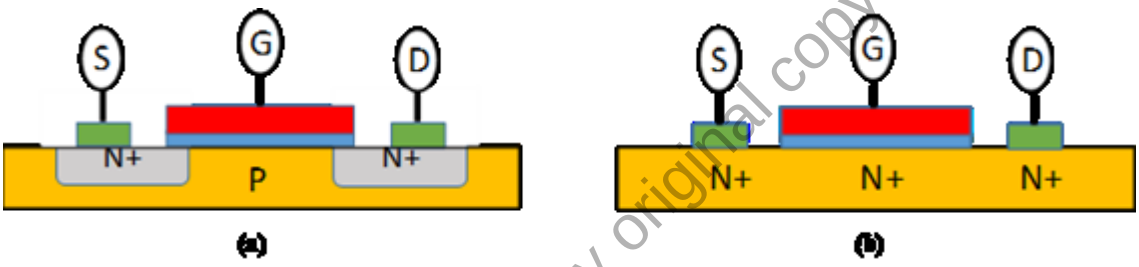

Figure 1.1: (a) Conventional transistor. (b) Junctionless transistor.

1.2.2 Problem Statement

Transistors are the elementary building blocks of the modern electronic devices where all the existing transistors such as bipolar junction transistor (BJT), field effect transistor (FET), MOSFET, and others have junction. Junction is occurring between the interfaces of oppositely doped semiconductor material. For an example, the opposite doping types in p-n junctions creates a depletion region naturally at thermal equilibrium. However, these transistors have faced several issues as the device is scaled down to nanometer regime. The fabrication of high quality junctions become more difficult as the transistors become smaller. This is because the manufacturing of high quality junctions becomes very expensive and difficult to be controlled since it requires several steps of lithography process. This problem becomes the main aspect that driving up costs in the IC manufacturing process.

Hence, the uses of thin effective oxide thickness (EOT) has been introduced because it can control threshold voltage (V_{TH}) roll-off as the channel length become shorter. Thin EOT is important as it will produce larger capacitance gate oxide and it will increase the on-state current of the transistor where the circuit speed tends to be maximized. Tunnelling leakage current becomes the most serious limiting factor for silicon dioxide (SiO_2) films thinner than 1.5nm. The chip oxide leakage current would be 10 A if an integrated circuit (IC) chip contains 1 mm^2 total area of this thin dielectric which SiO_2 leaks 103 A/cm^2 at EOT of 1.2 nm (Hu, 2009). Thus, the miniaturization has faced a significant challenge as it will lead to high current leakage, high power consumption, and lower the device performance as the number of transistors increases. Therefore, junctionless is easier and more saving in the IC manufacturing point of views.

1.2.3 Objectives

There are several objectives that can be achieved throughout this project as followed:

- To optimize the critical parameters in order to achieve full-depletion (parameters such as silicon thickness, width, gate workfunction, and dopant concentration will be considered in the simulation).
- To make the comparison between junctionless and junction transistors device performance in terms of digital figure-of-merits.
- To report the device performance on analogue and RF figures-of-merit between junctionless transistor (JLT) and junction transistor (JT).

1.3 Research Scopes

The aim of this research is to investigate the device performances of junctionless transistors over the conventional MOSFET. All devices in this project were simulated in 3-Dimensional (3D) images that have been performed by using Technology Computer Aided Design (TCAD) of Atlas simulator by Silvaco. The scope of this research work has been divided into four (4) main parts. The main parts are gate workfunction, silicon body width and thickness, and doping concentration. Before the research work can be properly conducted, the pre-work has been done to get the desired designated JLT and JT devices. The pre-work is the research based on other researchers, study the Atlas manual, and rewrite the coding until the desired designated JLT and JT devices have been achieved. Then, the research work can proceed to the main parts of the research scopes.

Firstly, the gate workfunction has been investigated throughout the simulation process for both devices. The mid-gap and high value of gate workfunction have been manipulated throughout the simulations process where the results have been analysed. Secondly, the silicon body width and thickness have been studied. These results have been analysed into electrical characterization and electron concentration. The digital figure-of-merits characterization such as threshold voltage, on- and off-state current, subthreshold swing, and drain induced barrier lowering has been applied throughout the analysis as an indicator of the device performances. In addition, the electron concentration has been analysed in order to investigate the device physics of the JLT and JT devices.

Thirdly, the doping concentration has been varied throughout the simulation process. The doping concentration is also important as the gate workfunction because it will huge effect to JLT device performance. Lastly, the device performance on analogue and RF figures-of-merit characterizations between JLT and JT down to 10 nm regime has

been reported. The purpose of this third research work is to know the downscaling limitation of this JLT device. Therefore, these research scopes are important as it would be used to analyse overall device performance of the JLT device over the conventional JT device.

1.4 Thesis Organization

This thesis has been organized into five (5) chapters. The chapters have been divided into background, literature reviews, methodology, results and discussions, and conclusion. Chapter 1 consists of researches rational, problem statements, objectives, and scopes. All these have been briefly written as the introduction or background towards this research. On the other hand, there were the theoretical parts of the device and others research that similar to this research in Chapter 2. Chapter 2 is important as it will give more understanding about the device and how to plan this research. Thus, the contents or knowledge in this chapter will be used in Chapter 4 later.

Besides that, Chapter 3 would be divided into four (4) parts. Firstly, there will be the introduction to the simulation tools which is TCAD Atlas Silvaco software that has been used throughout this research. Then, the JLT device architecture model has been explained in details by using the command scripts and the picture of the simulation model device. In addition, the simulated structures have been included in this chapter. Next, the electrical device characterization and data extraction methods have been explained in this chapter.

Moreover, there would be results and discussions in Chapter 4. The current-voltage characteristic curve would be generated and the other parameters such as threshold voltage (V_{TH}), on-state current (I_{ON}), off-state current (I_{OFF}), subthreshold slope (SS) and drain induced barrier lowering (DIBL) values were extracted. In addition to that, analogue

and radio frequency (RF) characterizations have been included in the results and discussions parts. These parameters are important as it will be used to analyse the 3D SOI JLT device performances. The conclusion and the recommendation would be discussed further in Chapter 5.

CHAPTER 2

LITERATURE REVIEWS

2.1 Introduction

This chapter elaborates the overview, to provide fundamental knowledge on MOSFET operation and the need of new device workfunction such as JLT. One knows that the size of MOSFET devices has been scaled down aggressively in these past few years due to the technology demand nowadays. There will be critical technology issues that must be overcome due to the scaled down of the MOSFET to nanometer regime. This critical issue is short channel effects (SCE) where it will hinder the MOSFET performances. Hence, it will minimize the power dissipation and the power supply voltages of this MOSFET device (Zhang, Zhao, Member, & Seabaugh, 2006).

2.2 Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

The transistor is very important as it is needed in almost electronic devices and systems nowadays. The transistor has been reformed year by year after the progression by John Bardeen, Walter Brattain, and William Shockley in 1947. It has become a turning point to a creation of smaller electronic devices even though J. E. Lilienfield's has patent the basic principle of FET in 1925. FET has plays an important role in human life as it is widely used in various fields that make human life become easier. Thus, the study of FET has been aggressively studied by another researcher as the principle of FET can be applied in various applications.