

Comparator Design Resistance Mitigation by using Cadence Virtuoso Tools in 45 Nanometer Process Technology

Abstract

This paper presents the resistance mitigation techniques for comparator design. Resistance plays an important role to semiconductor field. If resistance value higher than the design specification value, this might cause the electronic device burning and destroy. This project implements the techniques to mitigate resistance for the comparator design layout which are using multiple metal layers for routing, routing track improvement, increase metal width, increase number of vias and using higher metal layer for routing by using Cadence Virtuoso tools in 45 nanometer process technology. Based on the result, the total percentage for resistance mitigation for using multiple metal layers for routing is 73.66%, routing track improvement is 67.67%, increase metal width is 51.74%, increase number of vias is 50% and using higher metal layer for routing is 18.79%.

Keywords

45 nm process technology; Layout design; Resistance