

Design and Simulation of Cylindrical Stacked Silicon Nanowire (SiNW) Field-Effect Transistors

Abstract

In continuous effort to increase the current drive without sacrificing the off current and better off gate control on the channel, the MOSFET devices have advanced from classical, planar, single-gate and three-dimensional devices with multi-gate structures. Recently, multi-bridge-channel technology has become a feasible solution beyond FinFET multi-gate structure. In this work, we design Gate-All-Around (GAA) based on silicon nanowire. Numerical simulation based Silvaco Device tools has been used to design multiple number of cylindrical nanowires, then followed by different channel diameter, consisting of 20, 30 and 40 nm. The devices are characterized on transconductance, threshold voltage, DIBL and subthreshold slope. The simulation results indicate that the device performance is best at a nanowire diameter of 20 nm due to improved gate control over charge distribution. Regarding the number of nanowires, the voltage performance is not significantly affected by $N_{nw} = 1$ or higher. However, higher numbers of nanowires, such as $N_{nw} = 3$, demonstrate improved drain current and transconductance.

Keywords

FET; Nanowire; Simulation; Transfer Characteristics; Transistor