ANALYSIS AND DEVELOPMENT OF LOW THD SINGLE PHASE 11-LEVEL MULTILEVEL INVERTER

by

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TABLE OF CONTENT

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATION

AC	Alternating Current
DC	Direct Current
MOSFET's	Metal Oxide Semiconductor Field Effect Transistor
PV	Photovoltaic
THD	Total Harmonic Distortion
VRMS	Voltage Root Means Square
PWM	Pulses With Modulation

Analisis dan Pembangunan Penyongsang Fasa Tunggal 11 -Level Multilevel Inverter Dengan THD Rendah

ABSTRAK

Tenaga solar adalah alah satu tenaga yang boleh diperbaharui yang semakin mendapat tempat dalam menjana elektrik. Tenaga solar ditukarkan kepada arus terus (AT) menggunakan panel PV. Walaubagaimanapun, kebanyakan peralatan elektrik beroperasi menggunakan mod arus ulang-alik (AU),ini menyebabkan tenaga AT haruslah ditukarkan kepada bentuk AU. Sebuah penyongsang diperlukan untuk manjalankan penukaran tersebut. Penyongsang kawalan-PWM yang wujud mempunyai kadar pensuisan pada puluhan ribu *hertz* , dan ini menyebabkan kerugian yang tinggi dalam proses pensuisan sekaligus megurangkan kecekapan sesebuah system. Namun begitu, penyongsang bertingkat mampu beroperasi pada frekuensi yang lebih rendah dengan mengurangkan kerugian dalam pensuisan, yang mana meningkatkan kecekapan. Dalam kalangan topologi penyongsang bertingkat, penyebar jambatan-H bertingkat semakin mendapat tempat dalam penggunaan PV tenaga tinggi kerana struktur modula membolehkan voltan yang lebih tinggi beroperasi menggunakan piawai semikonduktor voltan rendah. Projek ini mengfokuskan kearah membina model, simulasi dan pembinaan prototaip sebuah penyongsang bertingkat jambatan-H 11 tingkat. Simulasi penyongsang bertingkat jambatan-H 11 tingkat dimodelkan menggunakan perisian PSIM. Walaubagaimanapun, sudut pensuisan 11 tahap ini haruslah dipilih secara sempurna supaya peningkatan keluaran AU menghampiri sinusoidal dapat dicapai. Justeru, empat teknik sudut pensuisan dinilai menggunakan simulasi. Keputusan simulasi menunjukkan salah satu daripada teknik penyusunan pensuisan dapat menghasilkan voltan keluaran yang mengandungi kandungan harmonik serendah 7.56%. Untuk mengesahkan keputusan simulasi, sebuah prototaip penyongsang bertingkat jambatan-H 11 tingkat telah dibina dan diuji. Keputusan eksperimen menunjukkan bahawa kandungan harmonic penyongsang tersebut ialah 7.56%, yang mana seiring dengan keputusan yang diperoleh daripada bahagian simulasi.

Analysis and Development of Low THD Single Phase 11-Level Multilevel Inverter

ABSTRACT

Solar energy is among the renewable energies that are gaining popularity for electrical power generation. Solar energy is converted into direct electricity (DC) using photovoltaic (PV) panels. Since most of the standard electrical appliances operate in alternating current (AC) mode, the DC electricity must be converted into AC form. An inverter is used to perform such function. Conventional PWM-controlled inverter is switched at tens of kilo-hertz range, and this will lead to high switching losses and reduced efficiency in the system. In contrast, a multilevel inverter can be switched at a much lower frequency and will produce lower switching losses and hence, higher efficiency. Among the multilevel inverter topologies, cascaded H-bridge multilevel inverter is gaining popularity for high power PV applications because the modular structure enables higher voltage operations using standard low-voltage semiconductors This project focuses on the modeling, simulation and hardware prototyping of a eleven-level cascaded H-bridge multilevel inverter. The simulation model of a eleven-level cascaded H-bridge multilevel inverter is modeled using PSIM software. However, the switching angles of the eleven-level cascaded H-bridge multilevel inverter must be properly selected so that a staircase AC output voltage waveform which is to a near sinusoidal waveform can be obtained. Therefore, four switching angle arrangement techniques are evaluated in the simulation. Simulation result show that one of the switching angle arrangement techniques is able to produce an output voltage waveform with harmonic contents as low as 7.56%. To validate the simulation result, a hardware prototype of the eleven-level cascaded H-bridge multilevel inverter was constructed and tested. The experimental result shows that the harmonic contents of the inverter is 7.56%, which corroborates with the simulation results.

CHAPTER 1

INTRODUCTION

1.1 Background

Solar energy is among the renewable energies that are gaining popularity for electricity generation because solar energy can be found in abundant quantity, always available and clean compared to fossil fuel and coal (Trabelsi & Ben-Brahim, 2011). Solar energy is converted into direct current (DC) electricity via solar panels, and this conversion process is known as photovoltaic (PV). It is common that the DC electricity is converted into alternating current (AC) so that it is compatible with most of the standard electrical appliances and the electrical grid system. An inverter is used to convert the DC into AC form (Daher et al., 2008). Many inverter topologies have been proposed by researchers in the past. Among them, multilevel inverter is gaining popularity because it is able to produce a sinusoidal-like staircase AC output waveform with low harmonic contents and therefore, does not require a bulky electrical filter to produce the sinusoidal waveform. (Adam et al., 2012; Cecati et al., 2010). Figure 1.1 show the sinusoidal waveform and stepped waveform. The blue color waveform is the complete one cycle sinusoidal waveform and the red color waveform is the complete one cycle for steeped waveform.

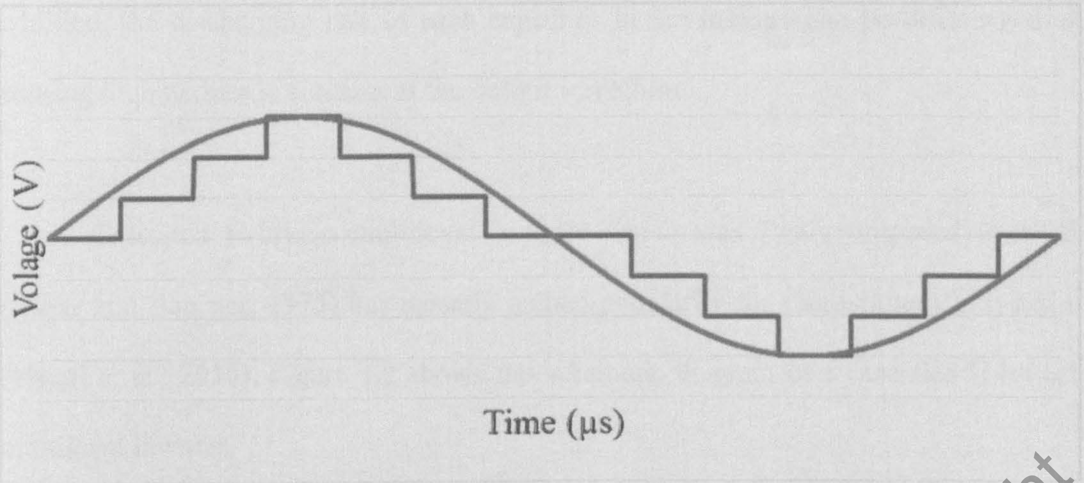

Figure 1.1: Sinusodial Waveform and Stepped Waveform

The common topologies of multilevel inverter are flying capacitor multilevel inverter, diode-clamped multilevel inverter, and cascaded H-bridge multilevel inverter with isolated direct current (DC) sources. Flying-capacitor multilevel inverter was firstly introduced in 1992 (Meynard & Foch, 1992). This topology uses a series of capacitors to hold the voltage levels from the DC sources to specific values and switches are controlled to produce the staircase output voltage waveform. Such topology suffers from a number of drawbacks. For example, the control scheme to balance the voltage in the capacitors is complicated and the number of capacitors that are required to construct the inverter is large when the number of voltage levels increases. The high number of capacitors will likely to give rise to reliability and failure issues. Diode-clamped multilevel inverter or also known as Neutral Point Clamped (NPC) inverter (Choi et al., 1991) was proposed in 1981. Similar to the concept of flying capacitor multilevel inverter, a series of capacitors and clamping diodes are used to clamp the voltage of the DC source to specific voltage levels. Such topology suffers from a few shortcomings. For example, the number of clamping diodes increases quadratically with the number of voltage levels, thus making the inverter bulky. In addition, the discharging rate of each capacitor in the inverter can be different, thus causing high harmonic contents at the output waveform

Cascaded H-bridge multilevel inverter which was firstly proposed in 1975 (Baker and Banister, 1975) has recently gained popularity for stand-alone PV systems (Najafi et al., 2010). Figure 1.2 shows the schematic diagram of a cascaded H-bridge multilevel inverter.

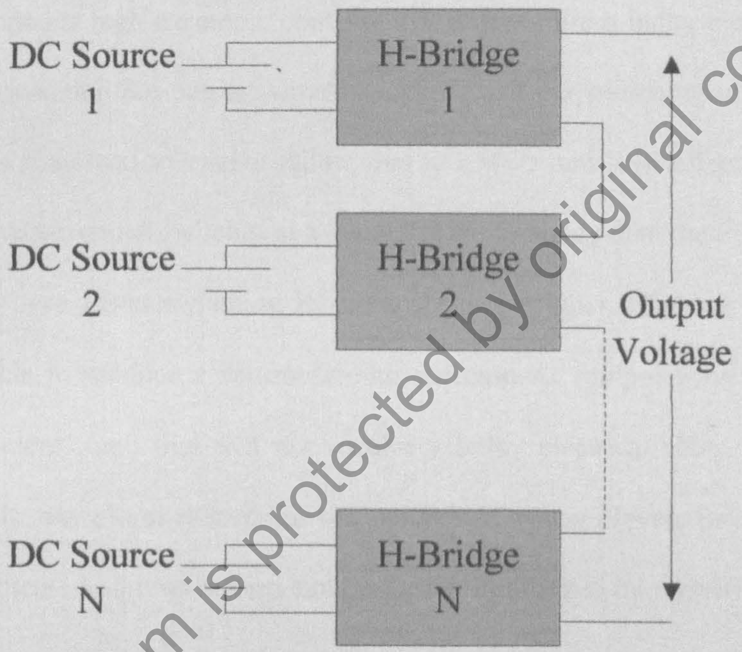

Figure 1.2: A cascaded H-bridge multilevel inverter

A cascaded H-bridge multilevel inverter is made up of a series connection of several single full bridge inverter module with separated DC sources. Examples of DC sources are solar cells, fuel cells, batteries, and ultra-capacitors. Such topology has a high degree of modularity because the number of output voltage levels can be easily adjusted by adding or removing the H-bridge. By connecting the H-bridges in series, this inverter has a voltage boosting capability and lowest voltage unbalance problem

(Sadikin et al., 2013). In the case of a faulty system, the faulty H-bridge can be easily traced and replaced.

1.2 Problem Statement

Conventional PWM-controlled inverter is switched at tens of kilo-hertz range, and this will lead to high switching losses and reduced efficiency in the system. In addition, the resulting output waveform is a train of pulses which suggest that the waveform contains high harmonic contents that will require a bulky electrical filter to produce a sinusoidal-like output waveform. The dv/dt per switching on the system is large and this may lead to system failure due to EMF's and EMI effect. In contrast, a multilevel inverter which switches at a much lower frequency than the PWM-controlled inverter will have lower switching losses and hence, higher efficiency. A multilevel inverter is able to produce a sinusoidal-like staircase AC output waveform with low harmonic contents, and this will not require a bulky electrical filter. The harmonic contents in the waveform reduces as the number of voltage levels increases, and the harmonic contents in the waveform can be further minimized by properly selecting the switching angles. Since the output waveform of a multilevel inverter consists of multi-stepped amplitudes, the dv/dt stress on the system is low and the electromagnetic interference caused by switching can be significantly reduced. Among the multilevel inverter topologies, cascaded H-bridge multilevel inverter is gaining popularity for high power PV applications because the modular structure enables higher voltage operations using standard low-voltage semiconductors.

1.3 Objectives

The objectives of this project are as follows:

i. To model and simulate a 11-level cascaded H-bridge multilevel inverter.

ii. To evaluate the harmonic contents of the voltage waveform produced by the 11-level cascaded H-bridge multilevel inverter under different switching angle arrangement techniques.

iii. To develop, construct and test a 11-level cascaded H-bridge multilevel inverter prototype.

1.4 Scope of Project

The scope of this project includes the simulation and hardware prototyping and testing of a 11-level voltage-source inverter. The simulation model of a 11-level cascaded H-bridge multilevel inverter will be modeled using PSIM software. Four different switching angle arrangement techniques will be evaluated using the modeled circuit. A hardware prototype of a 11-level cascaded H-bridge multilevel inverter using power MOSFETS as power switches will be designed and constructed. The harmonic contents of the output voltage of the constructed 11-level cascaded H-bridge multilevel inverter which are controlled using the four switching angles arrangement techniques will be evaluated experimentally and a comparison will be made.

1.5 Dissertation Synopsis

This report is divided into five main chapters, and the outline of each chapter is summarize as follows:-

Chapter one describes the background, problem statement, objectives and scopes of the project.

Chapter two presents the literature review of the project. In this chapter, the operation of various multilevel inverter topologies including the advantages and disadvantages are discussed. A comparison between the different multilevel inverter topologies is also made.

Chapter three details the methodology employed in this project, including modeling in PSIM software and hardware development. The operation of an 11-level cascaded H-bridge multilevel inverter is also described.

Chapter four presents, and discusses both the harmonic contents and efficiency obtained from both PSIM simulation and hardware testing of the constructed 11-level cascaded H-bridge multilevel inverter. A comparison of the THD and efficiency obtained from PSIM simulation and hardware testing is also made and presented.

Chapter five concludes the work of this project and proposes some future work.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter firstly discusses the operation of the three basic multilevel topologies which includes the diode-clamped multilevel inverter, flying capacitor multilevel inverter and cascaded H-bridge multilevel inverter with separated DC sources. The discussion focuses on the multilevel voltage-source inverters. Then, a comparison between these multilevel inverters such as the component counts is made. Lastly, the motivation of the selecting the cascaded H-bridge multilevel inverter topology is presented.

2.2 Flying Capacitor Multilevel Inverter

The first flying capacitor multilevel inverter proposed by Meynard and Foch in 1992 consists of three levels. Such multilevel inverter draws large attention for high power applications, for example, large motor drive and static power conditioners (Meynard et al., 1992). Flying capacitor multilevel inverters are commonly used for static VAR generation and static synchronous series compensator (SSSC) (Pharne et al., 2013; Shukla et al., 2004). Figure 2.1 shows a 5-level flying capacitor multilevel inverter. The circuit consist eight (8) power MOSFETs, six (6) balancing capacitors, four (4) DC-link capacitors and one (1) DC voltage source. Each capacitor ($C_1 - C_{10}$)

has a voltage VDC/4 across itself and the voltage across each power MOSFET is clamped to one capacitor voltage level i.e. VDC/4.

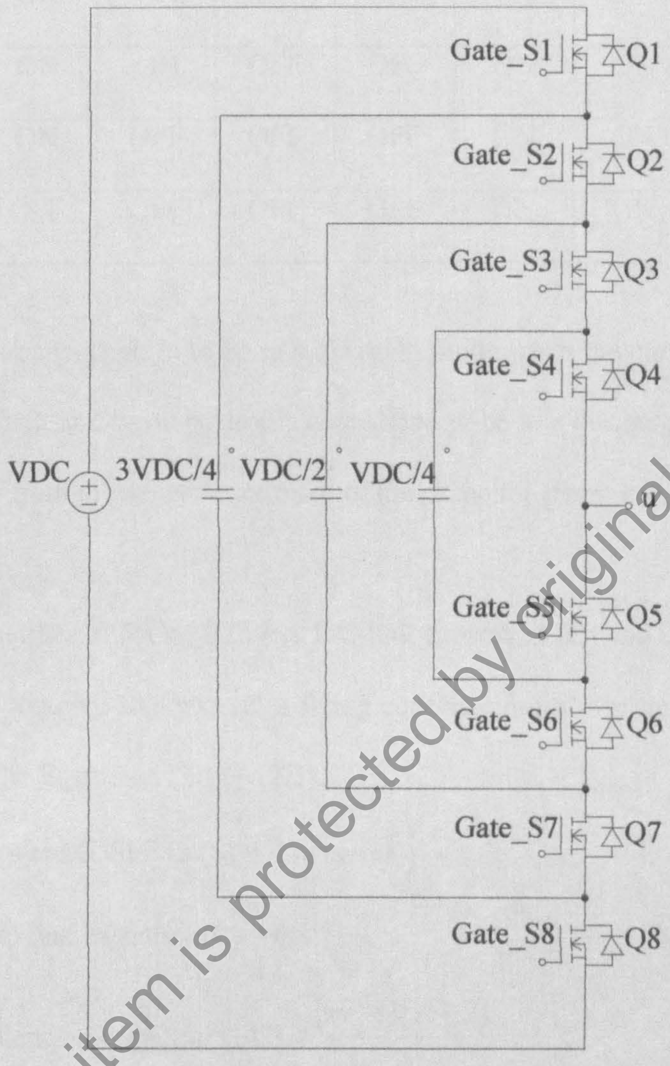

Figure 2.1: A 5-level flying capacitor multilevel inverter

Table 2.1 shows the possible switching sequences for switches (S_1 – S_8) that can be used to produce a 5-level staircase output voltage.

Table 2.1: Switching sequences of a 5-level flying capacitor multilevel inverter

Van	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
VDC/2	ON	ON	ON	ON	OFF	OFF	OFF	OFF
VDC/4	ON	ON	ON	OFF	ON	OFF	OFF	OFF
VDC	ON	ON	OFF	OFF	ON	ON	OFF	OFF
-VDC/4	ON	OFF	OFF	OFF	ON	ON	ON	OFF
-VDC/2	OFF	OFF	OFF	OFF	ON	ON	ON	ON

A capacitor is considered in to be in a charging mode when the current enters from the positive terminal, and the capacitor is considered to be in a discharging mode when the current enters from the negative terminal of the capacitor (Fang Lin, 2013).

The number of MOSFETs (S), DC-link capacitors (C) and balancing capacitors (BC) that are required to construct a flying capacitor multilevel inverter with m levels are given by the Equations (2.1) – (2.3).

Number of power MOSFETs (S) = $2\times(m-1)$ (2.1)

Number of DC-link capacitor (C) = $m-1$ (2.2)

Number of balancing capacitor (BC) = $\dfrac{(m-1)(m-2)}{2}$ (2.3)

2.2.1 Advantages of Flying Capacitor Multilevel Inverter

The advantages of flying capacitor multilevel inverter (Pharne et al., 2013; Shukla et al., 2004) are given as follows:

1. Real and reactive power can be controlled compare to diode-clamped inverter.
2. The capability of power storage is high because a large number of clamping capacitors are used.
3. The high number of capacitors enables the inverter to be operated in all sorts of duration and deep voltage sags.

2.2.2 Disadvantages of Flying Capacitor Multilevel Inverter

The disadvantages of flying capacitor multilevel inverter (Pharne et al., 2013; Shukla et al., 2004) are given as follows:

1. The voltages across all the capacitors are complicated to be measured.
2. Efficiency for real power transmission is poor.
3. The flying-capacitor inverter is more expensive and bulky compare to the cascaded H-bridge multilevel inverter.

2.3 Diode-Clamped Multilevel Inverter

The diode-clamped multileveled inverter which consists of 3-levels was first proposed in 1981 (Nabae et al., 1981) This topology has been experimental used by researchers for several applications such as variable speed motor drive and high voltage system interconnections (Jih-Sheng et al., 1995). Figure 2.2 shows the circuit of a 5-level diode-clamped multilevel inverter. The circuit consists of eight (8) power MOSFETs, twelve (12) clamping diodes, four (4) DC-link capacitors and one (1) DC voltage source (VDC). Each DC-link capacitor ($C_1 - C_4$) has a voltage VDC/4 across itself and the voltage across each power MOSFET is clamped to one capacitor voltage level through the clamping diodes.

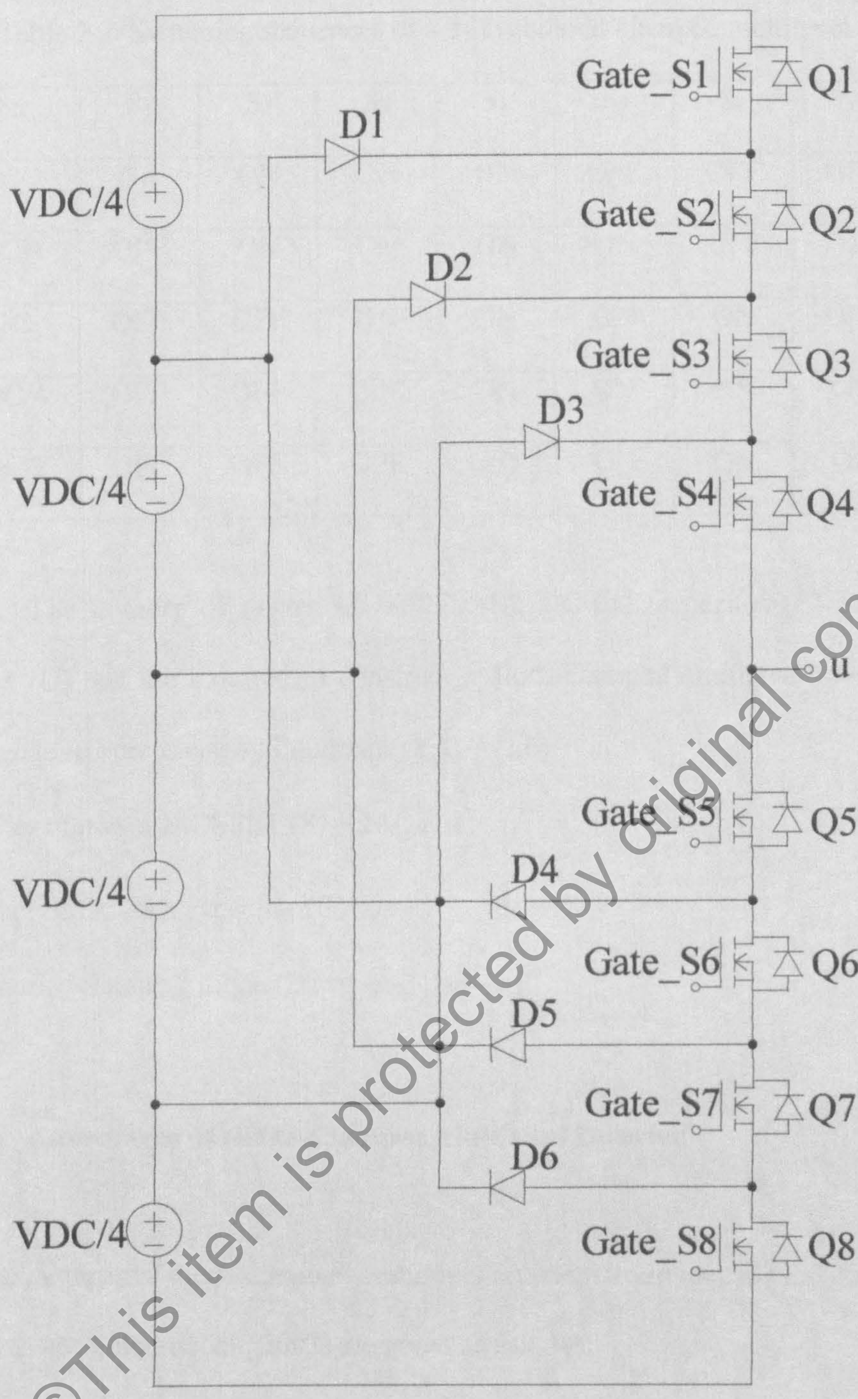

Figure 2.2: A 5-level diode-clamped multilevel inverter

Table 2.2 shows the switching sequences for switches (S_1 – S_8) that are used to produce a 5-level staircase AC output waveform.