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A 1.5 V, 0.85-13.35 GHZ MMIC low noise amplifier design using optimization technique

Abstract

This paper describes how a broadband, 1.5 V, 0.85-13.35 GHz low noise amplifier in 0.15 μm 85 GHz PHEMT process is synthesized to simultaneously meet multiple design specifications such as bandwidth, noise figure, power gain and power consumption. Power-constrained synthesis technique is used to design the broadband amplifier. The simulated peak S21 is 19.8 dB, maximum noise Figure is 2.5 dB, 3-dB bandwidth is 12.5 GHz and power consumption is 73.5 mW. The calculated Figure of merit (FOM) is better than many reported broadband low noise amplifier (LNA).

Keywords

Broadband amplifier; Integrated circuit; Monolithic microwave integrated circuit; Optimization; Power-constrained; Pseudomorphic high electron mobility transistor