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Implementation of LNS addition and subtraction function with co-transformation in positive and negative region: A comparative analysis

Abstract

The European Logarithmic Microprocessor (ELM) had been an outstanding breakthrough in logarithmic number system (LNS) research history. The processor successfully reaches the par ability of floating-point (FLP) processor with its rapid and accurate design towards FLP. The design was able to improve the LNS addition and subtraction procedure, which are the drawbacks of any implementation of LNS arithmetic. ELM's subtraction operation had adopted a unique approach, which is the first-order co-transformation to overcome the singularity-to-zero issue of the non-linear function in negative region. Therefore, this research had been introduced to extensively compare and analyze the ELM-based addition and subtraction procedures with the same co-transformation technique implemented in positive region. In achieving this, two aspects are considered, which are the accuracy towards FLP and the memory consumption of both procedures in both regions. Conclusively, the exact ELM-based implementation in positive region of both operations could be realized and achieved comparable accuracy and memory area with a slight modification of the operation procedure. The outcome of this analysis could benefit further investigation of optimizing the LNS design for hardware implementation.

Keywords

Addition; First order co-transformation; Floating point; Logarithmic number system; Positive and negative region; Subtraction