

DESIGN OF LC-QVCO IN 0.13 μm RF CMOS TECHNOLOGY

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1. Introduction

The quadrature Local Oscillator (LO) signal with low phase and amplitude error is a key element in many transceiver architecture which tend to dominate today's wireless communication technology, widely used in generating carrier signal for frequency translation. A VCO is also the heart of a frequency synthesizer circuit and a carefully designed VCO shows indispensable functions in transceivers. One of the most efficient schemes in RF modulation is Quadrature Amplitude Modulation (QAM) [1]. The adapted QAM modulation scheme, promotes the requirement in realizing a low power consumption and low phase noise topology.

The accuracy in reported QVCO architecture designed utilizing a RC-CR polyphase filter is strongly dependant on the on-chip component matching, whereas the usage of frequency divider in realizing the QVCO topology increases the power consumption and results in quadrature inaccuracy due to any asymmetry in the duty cycle of the master-slave D-flip flop based frequency divider [2]. A damping and tail resistor integrated cross coupled QVCO topology is exploited to enhance the phase accuracy [3], [4]. In this paper, the tradeoff between degradation of phase-amplitude and the ratio of coupling factor, K is appreciated with a penalty of physical mismatch [5]. The LC-QVCO architecture is realized in a complementary configuration, which is usually preferred in low-power applications as it exploits $\approx 50\%$ bias current reduction with double efficiency compared to the single coupled architecture.

A symmetrical Centre Tapped Inductor (CTI), [6] with underlying poly based PGS is designed and integrated into the QVCO architecture to provide frequency tuning via the LC tank configuration. The high Q, area efficient inductor is implemented and extracted utilizing ASITIC (Analysis and Simulation of Inductors and Transformer for IC's) tool. A multi-finger $3.124 \mu\text{m} \times 64 = 200 \mu\text{m}$ pMOS based varactor is integrated in the resonator tank to realize the frequency tuning. Both in accumulation and inversion region of operation the MOS capacitor exhibit a maximum oxide capacitance of, C_{ox} [7]. This chapter is organized as follows. The proposed QVCO circuit architecture is discussed in Section 2. Subsequently, Section 3 presents the simulation and measured results concerning the designed architecture. Finally, the conclusion is drawn in Section 4.

2.Circuit Architecture

2.1 Symmetrical Inductor

Figure 8.1(a) illustrates the layout view of the designed inductor with Patterned Ground Shield (PGS), which terminates the induced electric field and prevents it from reaching the substrate. Differential inductors have significant advantages over single ended inductors in silicon based on RFIC for higher Q factor and smaller size with a tradeoff of higher overall series and shunt capacitance, resulting in lower inductor self resonant frequency, f_{sr} [6]. Figure 8.1(b) describes the equivalent circuit model with PGS integrated, where $L_{DC+Eddy\ current}$ is the equivalent inductance due to the dc self inductance and mutual coupling inductance, R_{Metal} and $R_{Eddy\ current}$ denotes the dc metal line and reverse eddy current induction losses, respectively, C_s is the series capacitance due to the effect of interwinding and overlapping capacitance effect, whereas C_p and R_{shld} are the shield parasitic [8].