

DESIGN, FABRICATION AND  
CHARACTERIZATION OF CMOS ISFET  
FOR pH MEASUREMENTS

CHIN SENG FATT

UNIVERSITI MALAYSIA PERLIS  
2009

© This item is protected by original copyright



**DESIGN, FABRICATION AND  
CHARACTERIZATION OF CMOS ISFET  
FOR pH MEASUREMENTS**

by

**Chin Seng Fatt  
(0630110086)**

A thesis submitted  
in fulfillment of the requirements for the degree of  
Master of Science (Microelectronic Engineering)

**School of Microelectronic Engineering  
UNIVERSITI MALAYSIA PERLIS**

2009

## APPROVAL AND DECLARATION SHEET

This thesis titled Design, Fabrication and Characterization of CMOS ISFET for pH Measurements was prepared and submitted by Chin Seng Fatt (Matrix Number: 0630110086) and has been found satisfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the award of degree of Master of Science (Microelectronic Engineering) in University Malaysia Perlis (UniMAP). The members of the Supervisory committee are as follows:

**PROFESSOR DR. UDA BIN HASHIM**

Director

Institute of Nano Electronic Engineering  
University Malaysia Perlis  
(Head Supervisor)

**MOHD KHAIRUDDIN BIN MD ARSHAD**

Lecturer

School of Microelectronic Engineering  
University Malaysia Perlis  
(Co-Supervisor)

Check and Approved by

.....  
**(PROFESSOR DR. UDA BIN HASHIM)**

Director / Head Supervisor  
Institute of Nano Electronic Engineering  
Universiti Malaysia Perlis

(Date: .....)

School of Microelectronic Engineering  
Universiti Malaysia Perlis

2009

## Acknowledgements

I would like to thank University of Malaysia Perlis (UniMAP) and specifically School of Microelectronic Engineering for providing me with exceptional 2 years of trials and tribulations. Most of all, the excellent facilities are truly appreciated.

I wish to express sincere gratitude to project advisor, Professor Dr. Uda Hashim through whom that I have learned a lot and for his unfailing patience and guidance with regards to this project. I am also extremely thankful to Mr Mohd Khairuddin Md Arshad for giving a lot of advice and encouragements for my academic and research efforts.

It would have been impossible for me to complete my project without the help of the late Mr Phang Keng Chew and his wife, Ms. Nur Hamidah bt. Abdul Halim, Mr Hafiz b. Abd Razak, Mr Bahari Man, Mr Mohd Sallehudin Saad and Pn Shiela who have continuously aided in the successful completion of this project.

There are too many people to mention individually but some names stand out. I want to extend special thanks to doctoral candidates Pak Wahyu Hidayat and Pak Sutikno Md Nasri for their help and numerous suggestions at many occasions and being such good friends. Pak Wahyu and Pak Sutikno have always maintained a ready willingness to listen and help out in both personal and administrative affairs.

I thank my fellow colleagues of seniors and juniors at the Institute of Nano Electronic Engineering (INEE) and at the School of Microelectronic Engineering for sharing their time, expertise and humour with me. They are particularly Cikgu Kassim, Muzri, Emi, Shahrir, Azizul, Ikhwan, Maizatul, Naim, Syuhada, Ema, Rosyhidi, Siti Fatimah and Foo Kai Loong.

The financial support provided by the Ministry of Science, Technology and Innovation (MOSTI) and Government of Malaysia during 2007-2008 is hereby also acknowledged.

Last but not least, a very big thank you to my beloved family for their support, love and constant encouragement they have bestowed upon me. Without their support, I would never have gotten so far.

© This item is protected by original copyright

## Table of Contents

Declaration of Thesis	i
Approval and Declaration Sheet	ii
Acknowledgements	iii
Table of Contents	v
List of Tables	xi
List of Figures	xii
List of Abbreviations	xv
List of Symbols	xviii
List of Appendices	xix
List of Publications	xx
List of Awards	xxii
Abstrak	xxiii
Abstract	xxiv
<b>Chapter 1 Introduction</b>	<b>1</b>
1.1 Background of Research	1
1.2 Problem Statements	5
1.3 Research Objectives	7
1.4 Research Scopes	8
1.5 Thesis Overview	9

<b>Chapter 2 Literature Review</b>	<b>11</b>
2.1 Introduction	11
2.2 Ion Sensitive Field Effect Transistor (ISFET)	12
2.2.1 Basic Structure of an ISFET	12
2.2.2 The Operational Principle of the ISFET	13
2.3 Development of ISFET	19
2.3.1 Gate Materials	19
2.3.2 Encapsulation	21
2.3.3 Reference Electrode	23
2.4 Fabrication Technologies of ISFET	25
2.4.1 Standard CMOS Fabrication	25
2.4.2 Custom CMOS Fabrication	27
2.5 ISFET Simulation Model	28
2.6 Applications of ISFET	31
2.6.1 Ionic Measurements	31
2.6.2 Environmental Monitoring	32
2.6.3 Agriculture Field	34
2.6.4 Biomedical Field	35
2.6.5 Others and Future Applications	36
2.7 Chapter Summary	39
<b>Chapter 3 Process and Device Simulations of ISFET</b>	<b>40</b>
3.1 Introduction	40
3.2 Technology Computer Aided Design (TCAD)	40
3.2.1 Overview of Synopsys Taurus TCAD	41

3.2.1 Taurus TSUPREM4	43
3.2.2 Taurus MEDICI	43
3.3 ISFET Model in TCAD	44
3.4 Process Simulation of ISFET by Taurus TSUPREM4	45
3.4.1 Initial Structure Generation	46
3.4.2 Field Oxide Growth Simulation	47
3.4.3 Source and Drain Region Simulation	48
3.4.4 Gate Region Simulation	51
3.4.5 Silicon Nitride Deposition Simulation	53
3.4.6 Contact Region and Metallization Simulation	53
3.4.7 Formation of the Complete ISFET	54
3.5 Device Simulation of ISFET by Taurus Medici	55
3.5.1 Simulation of Gate Characteristics	56
3.5.2 Simulation of Drain Characteristics	57
3.6 Chapter Summary	58
<b>Chapter 4 CMOS ISFET Mask Design and Layout</b>	<b>59</b>
4.1 Introduction	59
4.2 ISFET Layout	60
4.3 Mask Fabrication Methodology	62
4.3.1 Mask Material	62
4.3.2 Mask Fabrication Set-Up	63
4.4 Results	64
4.4.1 N-Well Mask	64
4.4.2 Source Drain Masks	66

4.4.3 Gate Mask	67
4.4.4 Contact Mask	68
4.4.5 Metal Mask	68
4.5 Discussion	69
4.6 Chapter Summary	70

## **Chapter 5 ISFET Fabrication using CMOS Process** **71**

5.1 Introduction	71
5.2 CMOS Process Modules for ISFET Fabrication	71
5.2.1 Thermal Oxidations Modules	71
5.2.2 Photolithography Module	74
5.2.3 Wet Etch Module	78
5.2.4 Thermal Diffusions Modules	80
5.2.5 Thin Films Depositions Modules	80
5.3 CMOS ISFET Fabrication Details	83
5.3.1 Starting Material	83
5.3.2 Field Oxidation	84
5.3.3 N-Well Photolithography	86
5.3.4 N-Well Phosphorus Diffusion	88
5.3.5 N-ISFET Phosphorus Source Drain Formation	90
5.3.6 P-ISFET Boron Source Drain Formation	92
5.3.7 Gate Oxidation	93
5.3.8 Silicon Nitride Deposition	95
5.3.9 Nitride and Oxide Contact Via Etch	97
5.3.10 Metallization	99

5.4 Chapter Summary	102
---------------------	-----

## **Chapter 6 Functional Testing and Characterization of CMOS ISFET for pH**

### **Measurements 103**

6.1 Introduction	103
------------------	-----

6.2 Functional Testing of ISFET on Wafer Level	103
------------------------------------------------	-----

6.2.1 Measurement Set-Up	104
--------------------------	-----

6.2.2 Result and Discussion	106
-----------------------------	-----

6.2.2.1 $I_D$ - $V_D$ Characteristics of Al/Si <sub>3</sub> N <sub>4</sub> ISFET	106
----------------------------------------------------------------------------------	-----

6.2.2.2 $I_D$ - $V_G$ Characteristics of Al/Si <sub>3</sub> N <sub>4</sub> ISFET	108
----------------------------------------------------------------------------------	-----

6.3 Preparation of ISFET for pH Test	110
--------------------------------------	-----

6.3.1 Wafer dicing	110
--------------------	-----

6.3.2 Mounting and Wire Bonding	110
---------------------------------	-----

6.3.3 Encapsulation	111
---------------------	-----

6.4 Testing of ISFET in Aqueous pH Buffers	112
--------------------------------------------	-----

6.4.1 Experimental Set-Up	112
---------------------------	-----

6.4.2 pH Buffers	113
------------------	-----

6.4.3 Result and Discussion	114
-----------------------------	-----

6.4.3.1 $I_D$ - $V_D$ Characteristics of Si <sub>3</sub> N <sub>4</sub> ISFET	114
-------------------------------------------------------------------------------	-----

6.4.3.2 pH Sensitivity of Si <sub>3</sub> N <sub>4</sub> ISFET	118
----------------------------------------------------------------	-----

6.5 Chapter Summary	121
---------------------	-----

### **Chapter 7 Summary, Conclusions and Future Work 122**

7.1 Summary of the Thesis	122
---------------------------	-----

7.2 Conclusions	124
-----------------	-----

7.3 Suggestions for Future Work	126
References	128
Appendix A Publications	146
Appendix B Collaborations	148
Appendix C Awards	149
Appendix D Newspaper Clipping	150
Appendix E Synopsys Taurus TSUPREM4 ISFET Source Code	151
Appendix F Synopsys Taurus Medici ISFET Source Code	153

© This item is protected by original copyright

## List of Tables

Table	Description	Page
3.1	Process steps for ISFET simulation	45
5.1	Wet Etch Chemical Solutions.	79
5.2	PECVD Si <sub>3</sub> N <sub>4</sub> deposition recipe.	96
6.1	Measured V <sub>TH</sub> and sensitivity of ISFETs in three pH buffer solutions	118

© This item is protected by original copyright

## List of Figures

Figure	Description	Page
1.1	Litmus paper.	2
1.2	Typical pH Glass Electrode.	3
1.3	Author's impression of the first ISFET by Bergveld (1970).	5
2.1	Basic structure of an ISFET.	12
2.2	MOSFET and ISFET	13
2.3	Charge, field and potential profiles of ISFET	15
3.1	Overview of Synopsys Taurus TCAD	42
3.2	MNOS model and ISFET	44
3.3	The initial structure of the ISFET	46
3.4	The field oxide growth	48
3.5	The patterned source and drain region	49
3.6	The phosphorus concentration profile at the source and drain region	50
3.7	Phosphorus doping profile at $x=10$	50
3.8	Gate oxide growth	51
3.9	Phosphorus post dry oxidation	52
3.10	Phosphorus doping profile post dry oxidation	52
3.11	Silicon nitride deposition	53
3.12	Metal contacts patterning	54
3.13	The final structure of the ISFET with doping profile	55
3.14	Gate characteristics of n-channel metal-nitride gate ISFET	56
3.15	Drain characteristics of n-channel metal-nitride gate ISFET	57
4.1	ISFET layout	61

4.2	Design specifications of ISFET	61
4.3	Mask fabrication set-up	63
4.4	Design specification of N-Well region	65
4.5	N-Well mask layouts	65
4.6	n-ISFET source drain mask layouts	66
4.7	p-ISFET source drain mask layouts	67
4.8	Gate mask layouts	67
4.9	Contact mask layouts	68
4.10	Metal mask layouts	69
5.1	Oxidation furnace module	73
5.2	Filmetric F20 Thin Film Analyzer	73
5.3	Photolithography process flow	75
5.4	Wafer spinner	76
5.5	Hot plate	76
5.6	Contact Mask Aligner and Exposure System	77
5.7	Development Bench	77
5.8	Wet etch module	79
5.9	PECVD module	81
5.10	PVD module	82
5.11	Ambios XP-1 Stylus Surface Profiler	83
5.12	Silicon wafer	84
5.13	The cross section of the wafer after field oxidation	85
5.14	The cross section of the wafer after first photolithography process	88
5.15	The cross section of the wafer after n-well phosphorus diffusion	89

5.16	The cross section of the wafer after n-region source and drain formation.	91
5.17	The cross section of the wafer after p-region source and drain formation.	93
5.18	The cross section of the wafer after gate oxidation.	94
5.19	The cross section of the wafer after silicon nitride deposition.	96
5.20	The cross section of the wafer after contact via photolithography.	98
5.21	The cross section of completed CMOS ISFET (a) with metal gate, (b) without metal gate.	101
5.22	The actual completed CMOS ISFET wafer	101
6.1	The CMOS ISFET Semiconductor Characterization System (SCS) (a) Micro probe station (b) Keithley 4200 Semiconductor Parameter Analyzer	105
6.2	CMOS ISFET wafer level measurement set-up	105
6.3	The output characteristics of n-channel ISFET	106
6.4	The output characteristics of p-channel ISFET	107
6.5	Transfer characteristics of n-channel ISFET	109
6.6	Transfer characteristics of p-channel ISFET	109
6.7	Preparation of the ISFET from dicing till encapsulation	111
6.8	Graphic representation of the experimental set-up	113
6.9	pH buffer solutions from Thermo Scientific	114
6.10	Output characteristics of n-channel ISFET recorded in different pH buffers using the fixed biasing conditions ( $V_G=5V$ )	115
6.11	Output characteristics of p-channel ISFET recorded in different pH buffers using the fixed biasing conditions ( $V_G=5V$ )	115
6.12	Plot of the $V_G$ versus pH for ISFETs	119

## List of Abbreviations

Al	Aluminium
Al <sub>2</sub> O <sub>3</sub>	Aluminium Oxide
Ag/AgCl	Argentum/ Argentum Chloride (Silver/Silver Chloride)
BSC	Back sided contact
BOE	Buffered Oxide Etch
Ca <sup>2+</sup>	Calcium ion
ChemFET	Chemically modified field effect transistor
CMOS	Complementary Metal Oxide Semiconductor
CAD	Computer Aided Design
I-V	Current-Voltage
DIW	Deionised Water
DUT	Device Under Test
DC	Direct Current
FET	Field Effect Transistor
FIA	Flow injection analysis
HDL	Hardware Description Language
H <sup>+</sup>	Hydrogen ion
IGFET	Insulated Gate Field Effect Transistor
ISE	Ion sensitive electrode
ISFET	Ion Sensitive Field Effect Transistor
K <sup>+</sup>	Kalium ion
Hg	Mercury
Hg <sub>2</sub> Cl <sub>2</sub>	Mercury Chloride

MIS	Metal Insulator Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MNOS	Metal-nitride-oxide-semiconductor
MFCL	Micro Fabrication Cleanroom Laboratory
$\mu$ TAS	Micro total analysis system
$\text{Na}^+$	Sodium ion
NMOS	N-channel MOSFET
$\text{O}_2$	Oxygen (gas)
PMOS	P-channel MOSFET
PVD	Physical Vapour Deposition
PECVD	Plasma Enhanced Chemical Vapour Deposition
$\text{pCO}_2$	Power of carbon dioxide
pH	Power of hydrogen
PCB	Printed Circuit Board
QC	Quality control
RE	Reference Electrode
rpm	Revolution per minute
SCE	Saturated Calomel Electrode
SCS	Semiconductor Characterization System
SPA	Semiconductor Parameter Analyzer
Si	Silicon
$\text{SiO}_2$	Silicon dioxide or Silicon oxide or Oxide
$\text{Si}_3\text{N}_4$	Silicon Nitride
SPIICE	Simulation Program With Integrated Circuit Emphasis
$\text{SnO}_2$	Stannum oxide

Ta <sub>2</sub> O <sub>5</sub>	Tantalum penoxide
TCAD	Technology Computer Aided Design
TAT	Turn around time
VHDL-AMS	Very-High-Speed-Integrated-Circuit Hardware Description Language (VHDL)-Analog and Mixed Signal (AMS)

© This item is protected by original copyright

## List of Symbols

Symbol	Description	Unit
$I_D$	Drain current	A
$V_D$	Drain voltage	V
$V_G$	Gate voltage	V
$V_{TH}$	Threshold Voltage	V
$b$	Width of Area	$\mu\text{m}$
$L$	Length of Area	$\mu\text{m}$
$\mu_n$	Electron mobility in a channel	
$C_0$	Oxide capacitance per unit area	$\text{F}/\text{m}^2$
$V_{DSAT}$	Drain voltage at saturation	V

© This item is protected by original copyright

## List of Appendices

<b>Appendix</b>	<b>Description</b>	<b>Page</b>
A	Publications	146
B	Collaborations	148
C	Awards	149
D	Newspaper Clipping	150
E	ISFET TUSPREM4 Simulation Code	151
F	ISFET MEDICI Simulation Code	153

© This item is protected by original copyright

## List of Publications

- [1] U. Hashim and S. F. Chin, "Simulation of NMOS in Standard CMOS Process using Synopsys' TSUPREM-4 and MEDICI," in *Malaysian Technical Universities Conference on Engineering and Technology (MUCET)*, Universiti Teknologi Tun Hussein Onn, 2006, pp. 36-39.
- [2] S. F. Chin, U. Hashim, and M. K. Md Arshad, "CMOS ISFET Based pH Sensor using Si<sub>3</sub>N<sub>4</sub> Membrane: Towards Biomedical Application," in *International Conference on Advancement Materials and Nanotechnology (ICAMN)*, Langkawi, Malaysia, 2007, p. 176. (selected to be reviewed and published in American Institute of Physics(AIP), USA)
- [3] S. F. Chin, U. Hashim, and M. K. Md Arshad, "Development of N-Well CMOS Process in a University Microfabrication Laboratory," in *2nd Regional Conference on Engineering Education (RCEE)*, Persada Johor International Convention Centre, Johor Bahru, Malaysia, 2007, pp. 51 – 55.
- [4] U. Hashim, S. F. Chin, and M. K. Md Arshad, "Low Cost Mask Processing Technology Concept for Large Dimension ISFET Fabrication," in *Regional Symposium on Microelectronics (RSM) 2007*, Penang, Malaysia, 2007, pp. 150-152.

- [5] U. Hashim, S. F. Chin, M. K. Md Arshad, K. Abdul Rahman, and M. F. Mohd Yusof, "CMOS Based Sensors Research at UniMAP: CMOS ISFET," in *Malaysia Japan International Symposium on Advanced Technology (MJISAT) 2007*, Kuala Lumpur, Malaysia, 2007, pp. 345-347.
- [6] U. Hashim, M. K. Md Arshad, and S. F. Chin, "Development of CISFET Based Biosensor for Biomedical Applications," in *International Symposium on Olfaction and Electronic Noses (ISOEN)*, St. Peterburgs, Russia, 2007, pp. 136-137.
- [7] U. Hashim, M. K. Md Arshad, and S. F. Chin, "Modelling of Metal-Insulator-Semiconductor for Silicon Nitride ISFET Fabrication," in *2nd Malaysian Technical Universities Conference on Engineering and Technology 2008 (MUCET)*, Kangar, Perlis, Malaysia, 2008, pp. 94-96.
- [8] U. Hashim, M. K. Md Arshad, and S. F. Chin, "Silicon Nitride Gate ISFET Fabrication Based on Four Mask Layers using Standard MOSFET Technology," in *2008 IEEE International Conference on Semiconductor Electronics (ICSE)*, Malaysia, 2008, pp. 578-580.
- [9] U. Hashim, S. F. Chin, and S. Sakrani, "Application of Synopsys' Taurus TCAD in Developing CMOS Fabrication Process Modules," *International Journal of Nanoelectronics and Materials*, vol. 2, pp. 1-10, 2009.

## List of Awards

1. Research and Innovation Awards 2009 **Gold** Medalist
2. BioInno Awards 2009 **Silver** Medalist
3. PECIPTA 2009 **Silver** Medalist
4. Malaysia Invention and Innovation Awards 2009 **Silver** Medalist
5. BioInno Awards 2008 **Bronze** Medalist
6. Research and Innovation Awards 2008 **Bronze** Medalist

© This item is protected by original copyright

# REKABENTUK, FABRIKASI DAN PENCIRIAN CMOS ISFET UNTUK PENGUKURAN pH

## ABSTRAK

Transistor Kesan Medan Sensitif terhadap Ion atau lebih dikenali sebagai Ion Sensitive Field Effect Transistor (ISFET) ialah penderia pH jenis potentiometrik yang mudah diadaptasikan pada aplikasi kimia, bio-kimia dan bio-perubatan. Operasi ISFET ini berdasarkan penyerapan cas daripada larutan ujikaji pada antaramuka pepejal-elektrolit yang terletak di get ISFET. Hasilnya, voltan ambang ISFET dimodulasikan. Tesis ini menggambarkan rekabentuk, simulasi, fabrikasi dan pencirian ISFET untuk ukuran pH suatu larutan. Simulasi ISFET dijalankan terlebih dahulu dengan menggunakan perisian simulasi TCAD TSUPREM4 dan MEDICI. Fabrikasi ISFET dijalankan di dalam Makmal Bilik Bersih di Universiti Malaysia Perlis dengan menggunakan teknologi fabrikasi CMOS. Fabrikasi ini dapat dicapai oleh kerana kesesuaian teknologi antara ISFET dan CMOS. Silikon nitrida digunakan sebagai membran sensitive ion dan ia dilapiskan pada permukaan get dengan menggunakan teknik pemendapan wap kimia peningkatan plasma (PECVD). Sejumlah enam acuan direkabentuk dan digunakan dalam fabrikasi ini. ISFET yang difabrikasi bertujuan mengukur pH suatu larutan. Satu sistem pencirian semikonduktor yang terdiri daripada alat pengukur wafer mikro dan alat analisa parameter digunakan untuk mendapatkan pencirian yang jitu tentang ISFET. Bagi tujuan analisa ISFET dalam larutan, satu elektrod rujukan Argentum/Argentum Klorida dan tiga sample larutan penampakan dengan pH 4, pH 7 dan pH 10 masing-masing digunakan semasa eksperimen dilakukan. Kepekaan ISFET yang diukur ialah 40mV/pH bagi ISFET jenis n dan 30mV/pH bagi ISFET jenis p. Hasil yang diperolehi menunjukkan CMOS ISFET yang difabrikasi di makmal berfungsi seperti yang dijangkakan.