Design of High-Efficiency CMOS Class E Power Amplifier with Active Inductor for 5G Applications

by

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LIST OF ABBREVIATIONS

1G	First Generation
2G	Second Generation
3G	Third Generation
4G	Fourth Generation
5G	Fifth Generation
AI	Active Inductor
AR	Augmented Reality
BW	Bandwidth
C	Capacitive
CDMA	Code Division Multiple Access
CMOS	Complementary Metal-Oxide-Semiconductor
DAI	Differential Active Inductor
DAC	Digital-to-Analogue Converter
DC	Direct Current
DRC	Design Rule Check
DSP	Digital Signal Processing
EMI	Electromagnetic Interference
ERC	Electric Rule Check
GaN	Gallium Nitride
GHz	Gigahertz
GSM	Global System for Mobile Communications
IC	Integrated Circuit
IoT	Internet of Things
L	Inductor
LTE	Long-Term Evolution
LVS	Layout Vs Schematic
M	Transistor
MCMC	Malaysia Communications and Multimedia Commission
MHz	Megahertz
NMOS	N-channel Metal-Oxide-Semiconductor
P1dB	1dB Compression Point
PA	Power Amplifier
PAE	Power Added Efficiency

PEX	Parasitic Extraction
PMOS	P-channel Metal-Oxide-Semiconductor
Q-factor	Quality Factor
R	Resistive
RF	Radio Frequency
SoC	System on Chip
SP	Scattering Parameters
SRF	Self-Resonance Frequency
UMTS	Universal Mobile Telecommunications System
Vb	Biasing Voltage
VDD	Supply Voltage
VR	Virtual Reality
VSB	Bulk Voltage
VT	Threshold Voltage
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

LIST OF SYMBOLS

mW	Milliwatts
VDD	Supply Voltage
V	Voltage
V_{GS}	Gate to Source Voltage
V_{T}	Threshold Voltage
VSB	Bulk Voltage
V_{IN}	Input Voltage
I	Current
I_{IN}	Input Current
I_{BIAS}	Biasing Current
R	Resistor
Ω	Ohm
XL	Reactance
Z	Impedance
Z_{IN}	Input Impedance
j	Imaginary Unit
Im	Imaginary Impedance
Re	Real Impedance
C	Capacitor
Cgsn	N-Channel Gate-to-Source Capacitance
Cgsp	P-Channel Gate-to-Source Capacitance
ω	Angular Frequency
F	Frequency
Gv	Gyration Conductance
Q	Quality Factor
Q_{MAX}	Maximum Quality Factor
Qμ	Unloaded Q
QL	Loaded Q
PAE	Power Added Efficiency
gm	Transconductance
μm	Micrometer
nm	Nanometer
G	Gain
Gp	Power Gain
P_{OUT}	Output Power

P_{IN}	Input Power
P_{DC}	Consumed Power
P1dB	1dB Compression Point
Psat	Saturated Power
M	Moment Vector
W	Transistor Width
L	Transistor Length
Leq	Equivalent Inductance
nH	Nanohenry
dB	Decibel
dBm	Decibel-milliwatts
S_{11}	Input reflection coefficient
S_{22}	Output reflection coefficient
S_{21}	Forward transmission coefficient

Reka Bentuk Penguat Kuasa Kelas E CMOS Berkecekapan Tinggi dengan Pengaruh Aktif untuk Aplikasi 5G

ABSTRAK

Teknologi 5G telah mencapai kemajuan yang besar dalam beberapa tahun kebelakangan ini, terutamanya dalam kelajuan dan aplikasi. Mereka mempunyai kelajuan yang jauh lebih pantas berbanding teknologi 4G. Aplikasi ini memerlukan komponen dalam sistem penghantar terima yang boleh menghantar dan menerima maklumat melalui satu rangkaian. Salah satu komponen tersebut ialah penguat kuasa (PA), satu peranti yang boleh menguatkan isyarat. Walau bagaimanapun, kecekapan penguat kuasa adalah terhad pada frekuensi tinggi. Pengurangan dalam kecekapan peranti terutamanya berlaku kerana faktor kualiti rendah komponen yang membentuk reka bentuk litar. Faktor penyumbang paling teruk ialah induktor pada cip, yang boleh memenuhi sejumlah besar ruang dan mempunyai kesan yang paling besar pada peranti kerana kualiti faktornya yang rendah. Faktor Q yang rendah menjejaskan kecekapan disebabkan oleh kehilangan yang tinggi pada indukor lingkaran dalam cip. Objektif penyelidikan ini adalah untuk merekabentuk PA berkecekapan tambahan kuasa tinggi (PAE) untuk meningkatkan prestasi keseluruhan penghantar terima. Oleh kerana itu, induktor aktif (AI) berkualiti tinggi dicadangkan untuk menggantikan induktor lingkaran dalam cip pada litar PA untuk mengurangkan kehilangan dan seterusnya dapat meningkatkan kecekapan penguat kuasa. Induktor aktif yang dicadangkan mengguna struktur pembezaan sepenuhnya dengan cermin arus kaskod. AI direka bentuk dan disimulasikan dalam Cadence Virtuoso menggunakan teknologi Silterra CMOS 0.18 µm. Seterusnya, AI yang dicadangkan disepadukan dengan kelas E PA. Kelas E PA terdiri daripada dua peringkat iaitu peringkat pemandu dan peringkat kuasa kelas E. Simulasi bentangan pos menunjukkan bahawa induktor aktif mempunyai faktor kualiti tinggi 16,000 pada frekuensi 3.0 GHz, walau bagaimanapun faktor kualiti berkurang ke 500 pada frekuensi sasaran 3.5 GHz. Faktor Q pada frekuensi sasaran 3.5 GHz masih diterima untuk mengurangkan kehilangan. Seterusnya, induktor aktif ditambah pada rangkaian pemadanan keluaran PA untuk menggantikan induktor lingkaran dalam chip. Keputusan simulasi bentangan menunjukkan bahawa PAE meningkat daripada 67.33 % kepada 75.75 % apabila induktor lingkaran digantikan dengan AI. Begitu juga, PAE meningkat kepada 63.88 % daripada 50.6 % dalam simulasi bentangan pasca. Percanggahan antara bentangan pra dan pasca adalah disebabkan oleh kesan parasit. Pelaksanaan induktor aktif dengan ketara meningkatkan kecekapan PA bagi teknologi 5G.

Design of High-Efficiency CMOS Class E Power Amplifier with Active Inductor for 5G Applications

ABSTRACT

5G technology has made huge advancements in the past few years, especially in the speeds and applications. They have much faster speeds compared to 4G technology. These applications require components in their transceiver system, which can transmit and receive information through a network. One of those components is the power amplifier (PA), a device that can amplify the signal. However, the efficiency of power amplifiers is limited at high frequencies. The reduction in the efficiency of the device mainly happens because of the low Q-factor of the components that make up the design of the circuit. The worst contributing factors are the on-chip inductors, which can occupy a significant amount of area and have the greatest impact on the device due to their low Q-factor. The low Q-factor affects efficiency due to the high losses from the on-chip spiral inductors. The objective of this research is to design high power added efficiency (PAE) of PA to enhance the performance of the overall transceiver. Therefore, a high-quality active inductor (AI) is proposed to replace the spiral inductor in PA circuit to reduce losses and thus increase the efficiency of PA. The proposed active inductor employed a fully differential structure with a cascode current mirror. The AI is designed and simulated in Cadence Virtuoso using Silterra CMOS 0.18 µm technology. Further, the proposed AI is integrated with a class E PA. Class E PA consists of two stages, which are a driver stage and a class E power stage. The post layout simulation shows that the active inductor achieves a high-quality factor of 16,000 at 3.0 GHz frequency, however the Q factor is reduced to 500 at the targeted frequency of 3.5 GHz. The Q factor at targeted frequency at 3.5 GHz is still reasonable to reduce the losses. Furthermore, the active inductor is added to the output matching network of PA to replace the on-chip spiral inductor. The pre-layout simulation results indicate that the PAE is increased from 67.33 % to 75.75 % when spiral inductor is replaced by AI. Similarly, the PAE increased to 63.88 % from 50.6 % in a post-layout simulation. The discrepancy between pre and post layout is due to the parasitic effects.

CHAPTER 1: INTRODUCTION

1.1 Background

The evolution of the internet and mobile communication has been a phenomenal technological advancement. It first began in the 1980s with the introduction of the first generation (1G) and was mostly analogue. It allowed for voice calls over its network, but the area it covers had poor reception. The second generation (2G) began its inception in the early 1990s, which brought the Global System for Mobile Communications (GSM). With that addition, it brought functions such as text messaging and basic data services.

Afterwards, in the late 1990s and early 2000s, the introduction of the third generation (3G) it improved the data rates and mobile internet access (Shanzhi Chen et al., 2014). With technologies like the Universal Mobile Telecommunications System (UMTS) and Code Division Multiple Access (CDMA), this generation was able to use capabilities like video calls and mobile internet browsing.

Eventually, the late 2000s saw the introduction of the fourth generation (4G) (Govil & Govil, 2008). which as its previous gen, increased the data rate to a much higher extent. With it the use of mobile broadband was possible, bringing an era that allows for video streaming and online gaming using mobile phones. the leading technology was Long-Term Evolution (LTE), which had data rates up to 100 Mbps.

Currently, we are living in the 5G era, which started development in the early 2010’s (Pirinen, 2014) and first began spreading widely in the early 2020s. It brings many advantages to the table, such as a much higher data rate, significantly lower latency, and connecting many devices together simultaneously. The frequency ranges of such technology use a wide area including mm-Wave frequencies. It is expected that the technology will bring many new features and advancements like the augmented reality (AR), virtual reality (VR) and the internet of things (IoT).

Evidently, the technology of communications has evolved immensely in the past decades, with the emergence of the internet to the following generations that came after it. All of that in the last 3 decades. The latest strides in the technology have been the 5G (Fifth Generation), which increases the speed of the internet 100 times more than 4G (Fourth Generation) (Rao & Prasad, 2018). The main advantage of this increase in speed will give the Internet of Things-based technologies a more reliable connection with only a delay of one millisecond (Zhang et al., 2021) (Rappaport et al., 2013).

Furthermore, with every generation of the internet comes a new frequency spectrum, the comparison made in (Ahmed et al., 2015) shows that. If we look at older technologies like 3G, the frequency range reaches a maximum of 2100 MHz, while 4G reaches 2.5 GHz. The 5G technology can go much higher than the 56 GHz range. Yet, CMOS technology reaches a limit with higher frequencies as seen in (Lie et al., 2018), (Chappidi et al., 2020), (Asbeck et al., 2019), since it is quite difficult to design a high frequency device without reducing the transistors size (Radamson et al., 2020), and thus reducing the power of the transistor to increase the frequency spectrum.

Moreover, the frequency ranges for 5G communications are either sub-6 GHz for lower spectrum or mm-wave signals at the end of it (Al-Falahy & Alani, 2017). The development of the lower spectrum is due to higher losses from the fact that the path has higher carrier counts in mm-Wave compared to the sub-6 GHz (Niu et al., 2015) This might have improved in the past few years, but as we see in (Hasan et al., 2020), developing an amplifier for the system is still not efficient compared to the lower range of frequencies.

In Malaysia, 3.5 GHz is the main frequency range according to the Malaysia Communications and Multimedia Commission (MCMC), as stated in the official press release (Parliament et al., 2020) in January 2020, the document states that the frequency range is from 700 MHz to 3.5 GHz for sub-6 GHz frequencies, and at 26 GHz to 28 GHz for mm-Wave frequencies.

Thus, designing a radio frequency (RF) system suitable for that frequency range, it begins at the transceiver, where the block diagram of the device represents the front end for RF systems (Levinger, 2015). The transceiver functions as both a transmitter and a receiver, combining their roles. In Figure 1.1, the block diagram illustrates these components. The transmitter converts the digital signal to analogue, modulates it, combines it with the mixer, and amplifies it using a power amplifier to transmit over distances. The receiver amplifies weak incoming signals with a low-noise amplifier, processes them through the mixer, demodulates them, and converts them back to digital format.

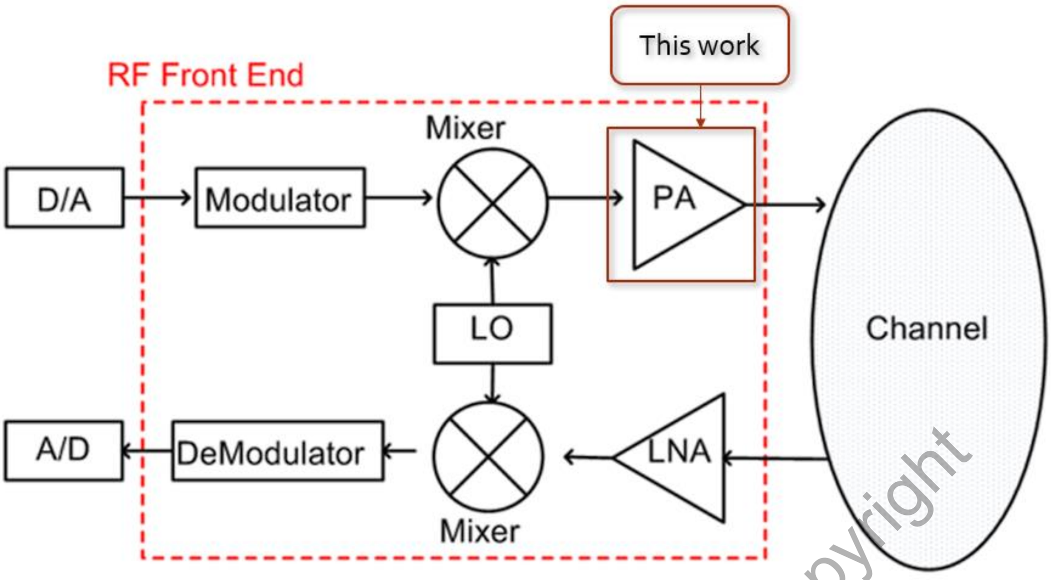

Figure 1.1 Simplified RF front end transceiver block diagram (Levinger, 2015).

An essential part of RF systems, the power amplifier (PA) transforms direct current (dc) input power into a significant output power in the radio frequency (RF/microwave) range. In contrast to a basic small-signal amplifier that is driven to saturation, a power amplifier comprises a variety of methods that go beyond simple linear amplification. With ancillary circuits like modulators, frequency converters, signal generators, signal processors, linearizers, and power supplies coexisting with them, PAs are essential components of transmitters (Raab et al., 2002).

What's more, there are many classes for power amplifiers, depending on their functionality and applications, some focus more on linearity, which basically focuses on the high output of the device, while switch-mode amplifiers are more on efficiency (Gong et al., 2006). These can be class-A, class-B, and class-C for linear mode. While class-D, class-E and class-F for switch mode.

Consequently, the biggest component in power amplifiers is the inductors, the implementation of them in an on-chip design proved much difficult because of the power delivery, EMI sensitivity and other factors (Gardner et al., 2009). The usual inductor type is a passive component that controls electric current as magnetic fields. While there are other inductors that have active components that mimic this behaviour, it is usually based on the required design weather it is required for linearity or efficiency (Patel, 2017).

So, to improve the power-added efficiency in the power amplifier, the design of better quality factor components could prove beneficial—specifically, the inductors when paired with RF design systems.

1.2 Problem Statement

The allocation of the 3.5 GHz spectrum band for 5G mobile broadband services within Malaysia, marks a significant advancement in wireless communication. This move aligns with the global trend of utilizing higher-frequency bands for 5G networks. The 3.5 GHz spectrum band offers the potential for significantly enhanced data speeds and reduced communication delays, which are pivotal for the success of 5G networks in Malaysia. This allocation represents a fundamental building block for enabling the promised benefits of the 5G wireless revolution in the country.

In 5G systems, the transmitter, including the power amplifier (PA) and related components, plays a vital role in converting digital data into RF signals for high-speed data transfer, low latency, and connectivity. However, as technology evolves and becomes more widespread, one of the challenges that engineers and designers face is the efficiency of power amplifiers (PAs). PAs play a crucial role in wireless devices as they are responsible for amplifying signals for transmission. Historically, PAs have been notorious for their inefficiency, often operating at less than 50% efficiency (Ginzberg & Cohen, 2022; Yi et al., 2021a; Zhang et al., 2021). This inefficiency not only results in higher energy consumption but also leads to the generation of excessive heat, which can be problematic for device performance and longevity.

To address the pressing issue of PA inefficiency, designers are focusing on improving the quality of passive electronic components, particularly inductors. In this context, the Q factor becomes a central consideration. The Q factor is a measure of component quality and is relevant in two distinct forms: unloaded Q (Qµ) and loaded Q (QL). For efficient PA design, it is imperative that the Qµ of components, especially inductors, significantly exceeds the QL. This discrepancy minimizes resonant losses, which can have a substantial impact on overall efficiency.

A crucial aspect of the efficiency puzzle lies in choosing between spiral inductors and active inductors. While spiral inductors may occupy more physical space on the chip and have a much lower quality factor, they tend to exhibit higher linearity compared to their active counterparts. This consideration often makes spiral inductors the preferred choice for achieving higher power gain in power amplifier designs. By optimizing component quality, minimizing losses, and exploring advanced component options, the objective is to push PA efficiency beyond the 50% threshold. Achieving this goal conserves energy and ensures the reliable and efficient operation of 5G devices, contributing significantly to the success of 5G wireless communication systems in Malaysia and globally. However, the design of AIs for power-hungry devices like the power amplifier could prove difficult. Since it will also increase the power consumption of the overall device. That is mainly due to the active nature of the device itself and how much it needs to function properly at high frequencies.

1.3 Research Objective

The research objectives for this work are as follows:

1. To investigate a method for designing a high-quality factor active inductor.

2. To design high quality (Q) factor of active inductor using 0.18 µm CMOS technology, targeting a Q-factor of approximately 300 or higher.

3. To validate the functionality and performance of the proposed active inductor in a class E power amplifier circuit.

1.4 Research Scope

The scope of this work is limited to the design schematic, simulation, design layout and perform post-layout simulation. The design technology is utilizing Silterra CMOS 0.18-µm process. The proposed design is targeted at frequency of 3.5 GHz which the low frequency band for 5G technology. This has been chosen by the Malaysian telecommunication company as the standard for lower frequency range 5G internet connection.

The core tools employed in this research encompass the Cadence Virtuoso software suite a comprehensive and essential toolkit for integrated circuit design. Virtuoso facilitates intricate schematic design, precise layout editing, and offers advanced simulation capabilities. By utilizing both the layout and schematic editors within Virtuoso, this research can meticulously create and evaluate the power amplifier design. Importantly, Virtuoso supports simulations at various stages of design, including pre-layout and post-layout, providing a comprehensive view of circuit performance. The simulation will focus on linearity from s-parameters to stability taken from K-factor and lastly the PAE that is the main goal. All those tests will be done in both pre- and post-layout.

A systematic simulation approach is fundamental to this research. It involves conducting analyses to the s-parameters, PAE, linearity, and stability, to determine optimal parameters, ensuring a balanced design that combines efficiency and performance. Additionally, the creation of a netlist, a foundational element in electronic design, allows for validation, ensuring the physical implementation aligns with the schematic design.

The crux of this research lies in the evaluation of the PA’s performance. This entails conducting both pre-layout and post-layout simulations, enabling a comprehensive understanding of the circuit's behaviour under various operating conditions. Furthermore, a comparative analysis with prior CMOS technology works is planned, serving as a benchmarking exercise to identify potential innovations or refinements in the approach. Such a comparison carries significant implications for the field of power amplifier design in integrated circuits.

1.5 Thesis Organization

The thesis structure is as follows; it starts with the introduction in chapter 1, which show the background of the project and discusses the motivation of this research along with the problem statement, objectives, and thesis organization.

Chapter 2 will discuss the literature review of the project, that focuses on the development of the inductor and its role in the power system block diagram, its limitations and how to improve them when used in the power amplifier design and its structure.

Then we move to the design technique and method, for quality factor improvement of the active inductor, which will improve the efficiency of the power amplifier in chapter 3. The measurement style and design structure of both devices will be discussed there.

In chapter 4, the results of the simulation in both pre- and post-layout for both devices will be discussed, specifically at 3.5 GHz. The performance of the AI and PA is measured upon certain parameters that were defined in the previous chapter.

Finally, a summary and conclusion for the whole study will be made in the final chapter, with the addition of ways and suggestions to improve the design even further in the future.