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Design and characterization of a 3.5 GHz CMOS Power amplifier for low-band 5G applications

Abstract

A 3.5 GHz CMOS power amplifier (PA) designed for 5G applications is presented in this study, utilizing the 0.18 µm RF CMOS process technology. The circuit architecture comprises two stages: the first stage employs a cascode topology with a negative voltage applied to the transistor body technique to achieve sufficient gain and minimize current, thereby reducing power consumption. In the second stage, to ensure high efficiency, a class-E amplifier is being used. Measurement results indicate a power gain (S_{21}) of 17.2 dB, a power-added efficiency (PAE) of 45.6% and a saturated power (P_{sat}) of 8.5 dBm, obtained at 3.5 GHz. These findings validate the suitability of the proposed design at low-band frequency for 5G applications. The chip area for the proposed design is 2.45 mm^2. The discrepancy between simulation and measurement is due to the parasitic in the layout design.

Keywords

CMOS; High efficiency; Power amplifier; Power-added efficiency; Radio frequency