Design and Analysis of 90 nm Two-Stage Operational Amplifier Using Floating-gate MOSFET

by

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LIST OF ABBREVIATIONS

IC	Integrated Circuit
RF	Radio-Frequency
CMOS	Complementary-Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor-Field-Effect-Transistor
V_t	Threshold voltage
FGMOS	Floating-gate MOS
Op-amp	Operational amplifier
HF	High Frequency
EEPROM	Electrically Erasable Programmable Read-Only Memory
EPROM	Erasable Programmable Read Only Memory
FG	Floating Gate
Poly1	First Polysilicon
Poly2	Second Polysilicon
VCVS	Voltage Controlled by Voltage Sources
Q_{FG}	Residual Charge
EDA	Electronic Design Automation
SoCs	Systems-on-Chips

LIST OF SYMBOLS

ε_{SiO_2}	Permittivity of the silicon dioxide.
β	Transconductance parameter
μ_n	Electron mobility
μ_p	Hole mobility
λ	Channel-length modulation parameter
ρ	Pole

Rekabentuk dan Analisa Dua-Peringkat Litar Penguat Kendalian 90nm Menggunakan Get-Terapung MOSFET

ABSTRAK

Voltan rendah, lesapan kuasa rendah, gandaan tinggi dan padanan adalah sebahagian dari pertimbangan ketika merekabentuk satu litar analog. Suatu voltan paling rendah boleh meningkatkan jangka hayat bateri dan ketumpatan integrasi seperti permintaan pasaran. Get-terapung Separuh-Pengalir-Oksida-Logam (MOS) juga dikenali sebagai FGMOS adalah rekabentuk teknologi baru yang diperkenalkan sebagai satu elemen dalam rekabentuk litar voltan rendah dalam teknologi CMOS. Teknik FGMOS telah dilaporkan sebagai aplikasi litar voltan rendah dan rekabentuk kuasa rendah untuk meningkatkan jangka hayat bateri disebabkan voltan ambang yang lebih rendah. Masa operasi transistor FGMOS boleh ditingkatkan dengan mengawal voltan ambang tanpa mengurangkan saiz transistor tersebut. Kajian ini menumpukan kepada menganalisa dan membuat perbandingan simulasi aplikasi teknik FGMOS dengan MOSFET yang lazim untuk pelbagai litar. Nisbah kapasitor 0.5 dengan nilai 2 fF bagi transistor FGMOS telah dipilih bagi mendapatkan keputusan keluaran yang paling stabil. Litar penguat kendalian FGMOS yang dicadangkan mengandungi dua peringkat yang dinamakan litar kebezaan masukan dan peringkat penimbal keluaran yang menyumbang kepada penggandaan signal masukan. Simulasi litar dianalisa dengan menggunakan perisian Full Custom Synopsys dengan teknologi CMOS 90 nm. Keputusan simulasi menunjukkan kira-kira 42 dB gandaan dengan 3dB-lebar jalur sebanyak 233 kHz, unit gandaan lebar jalur sebanyak 23.6 MHz dan jumlah kuasa lesapan sebanyak 203.3520 mW. Sebagai kesimpulan, cadangan rekabentuk FGMOS menunjukkan keputusan setanding dengan rekabentuk MOSFET yang lazim. Bagaimanapun, prestasi cadangan rekabentuk boleh diperbaiki dalam kajian lanjut disebabkan voltan batasan yang lebih rendahnya.

Design and Analysis of 90nm Two-Stage Operational Amplifier Using Floating-gate MOSFET

ABSTRACT

Low voltage, low power dissipation, high gain and matching are some of the concern when designing an analog circuit. A very low voltage can increase battery lifetime and integration density as market demands. Floating-gate Metal-Oxide-Semiconductor (MOS) also known as FGMOS is a new technology design that has been introduced as an element in low voltage circuit design in CMOS technology. FGMOS technique has been reported as low voltage and low power design application for increasing the battery lifetime due to its lower threshold voltage. The operational time of the FGMOS transistor can be improved by controlling the threshold voltage without reducing the feature size of the transistor. This research focuses on analyzing and comparing the simulation application of FGMOS technique with conventional MOSFET for various circuit designs. Capacitor ratio of 0.5 with value of 2 fF of the FGMOS transistor is chosen in order to have most stable output result. Proposed FGMOS operational amplifier circuit consists of two stages namely input differential circuit and output buffer stage that contributes in amplifying an input signal. The circuit simulations are analyzed using Full Custom Synopsys software with 90 nm CMOS technology. The simulated results show approximately 42 dB of gain with 3dB-bandwidth of 233 kHz, unity gain bandwidth of 23.6 MHz and total power dissipation of 203.3520 mW. In conclusion, the proposed FGMOS designs show comparable result with conventional MOSFET designs. However, the proposed design performance can be improved in further research due to its lower threshold voltage.

CHAPTER 1

INTRODUCTION

1.1 Overview

Analog Integrated Circuit (IC) design is one of the broad categories in IC design instead of digital IC design. Analog IC design is specialized in designing power IC such as a low power Complementary-Metal-Oxide-Semiconductor (CMOS) acquiring multichannel signals design of neural activities (Deepika, 2015). Another application of analog IC is in Radio-Frequency (RF) or microwaves such as ultra-wideband low noise amplifier for wireless communication in transporting voice which is widely used nowadays (Yousef, 2013).

Researchers are now struggling in finding a very low voltage for increasing the battery lifetime and integration density due to market demands. Low voltage, low power dissipation, high gain and matching are some of the concern when designing analog circuit. Almost all portable electronic devices use a battery as their power supply (Stephen Kosonocky, 2008).

The threshold voltage (V_t) is the main factor that is focused to be as minimum as possible. Basic MOSFET has a disadvantage where it has a quite high V_t, meaning that the device has to take a longer time to turn on or operate. In op-amp application, the use of Floating-gate MOS (FGMOS) would increase the operating range of op-amp through programming the threshold voltage of the FGMOS (M. B. K Jamal, 2012).

FGMOS device is widely used for improving the analog circuit accuracy such as a multiplier. It also can be used in analog memory elements, part of the capacitive biased circuit also as adaptive circuit elements due to its low voltage and low power. The operational time of an FGMOS can be improved by controlling the V_t without reducing the feature size (Abirami, 2014).

Operational amplifier (op-amp) is a device used to amplify the small signals, for addition or subtraction voltages, and in active filtering. During designing the circuit, it must have a high gain, low-power or low-current and can function over various frequencies as designed by Sajid, 2016. The idea for this research is to design an op-amp by applying the FGMOS transistor. Comparisons have been made by Wairya and she concludes that by applying this technique, it leads to a significant increase in DC gain and decrease in the settling time without extra power consumption (Wairya, 2015).

1.2 Problem Statement

CMOS technology offers high density and consumes low power for analog circuit development. Nevertheless, reducing power and increasing the lifetime of battery operated circuits, the CMOS technology requires voltage scaling ability. Besides, the operation of circuits at low power supply voltage poses constraints of apparatus noise level and V_t.

There are a few outline procedures for acknowledging the low power and low voltage analog circuits. FGMOS design has been introduced to overcome the problem in CMOS technology. Therefore, the FGMOS transistor is used as an element in low voltage circuit design. It overcomes the arising problem due to high V_t in accomplishing low voltage circuits. Besides, it offers advantage of lower V_t without scaling the device due to its unique feature.

1.3 Research Objectives

The main objective of this research is to design and compare the characteristic of two-stage op-amp by applying the basic MOS transistor and FGMOS transistor using 90 nm technology. Specific objectives of this research are listed as below:

i. To analyze the characteristic of basic MOSFET and FGMOS transistor for current mirror design.

ii. To analyze the characteristic of basic MOSFET and FGMOS transistor for differential amplifier design.

iii. To design and compare the performances and characteristics of two-stage op-amp using basic MOSFET and FGMOS transistor.

1.4 Scope of Project

This dissertation presents the development of two-stage op-amp using FGMOS technology. The design is simulated at High Frequency (HF) band which is in between 3 MHz to 30 MHz. The transistors used in this design are based on 90 nm process technology. First, the related circuit single NMOS, current mirror and differential amplifier are simulated as an initial analysis before it was proceed with two-stage op-amp design based on referral journal. Then, further analysis is carried out with input MOSFET for two-stage op-amp design which was replaced by FGMOS transistor. Last, the circuits' performances are compared and analyzed. All circuits are simulated using Full Custom Synopsys software.

1.5 Structure of Dissertation

This dissertation is structured into several chapters covering different aspects of the research. An overview of each chapter is described as follows:

Chapter 1 presents an introduction of the op-amp circuit followed by an overview of MOSFET and FGMOS transistor. The problem statement, main objectives and scopes of the research are also included in this chapter.

Chapter 2 addresses the literature review of FGMOS basic structure and the large signal analysis of FGMOS transistors. Figures of merit for the MOSFET and FGMOS transistor such as the V_t, the amount of current flow and the power consumption are analyzed. The concept of the current mirror, a differential amplifier, and op-amp are also discussed in this chapter. Finally, a brief introduction on simulation tool used in this research is presented.

Chapter 3 discusses the methodology for this research. The specifications of the design are addressed, before commences with a discussion of the op-amp using basic MOSFET and FGMOS transistor.

Chapter 4 presents the designs and analysis of the op-amp using all criteria discussed in Chapter 2 and Chapter 3. The verification and validation of all designs are compared and analyzed using standard library available in Full Custom Synopsys software.

Chapter 5 summarizes the work discussed in the earlier chapters. Future reccomendations to improve the designs performance are also suggested in this chapter.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Based on the problem statement, a few simulation and analysis application circuits need to be analyzed to design the two-stage op-amp. First, the overview of the FGMOS transistor against conventional MOSFET includes its advantages and review of the n-input structure of FGMOS over the conventional MOSFET are studied and discussed. Next, the techniques of implementation circuit for two-stage op-amp such as bias circuit, differential amplifier circuits, gain circuit and compensation circuit are analyzed. Also, a comprehensive literature review of different journals are deliberated to obtain the information thus provides critical evaluation about this research.

2.2 Floating-gate MOSFET (FGMOS)

2.2.1 Overview of FGMOS

A multi-terminal structure transistor known as FGMOS application first reported in the year 1967 for both analog and digital circuit. It is widely used for storing data like Electrically Erasable Programmable Read-Only Memory (EEPROM), Erasable Programmable Read Only Memory (EPROM) and FLASH memories due to its advantage in long-term non-volatile information storage devices (Sze, 1967). It is a non-volatile type memory which will retain data in the absence of a power supply such as EEPROM.

Floating-gate MOS is a transistor that has a similar structure with the conventional MOSFET. The different of this transistor against the conventional transistor is its gate is electrically isolated that making no resistive connection to the gate. Inputs are deposited above the Floating Gate (FG) and are electrically isolated from it. The inputs are capacitively connected to the FG. The FG is entirely enclosed by the highly resistive material and it defines the DC operating point of the FGMOS (Rodriguez-Villegas, 2006).

The structure of this typical n-type FGMOS transistor is illustrated in Figure 2.1. The FG is surrounded by two insulator layers, SiO_2. The first polysilicon (poly1) is a layer that extends outside the active area and the second polysilicon (poly2) are placed on top of the upper SiO_2 insulating layer (Rodriguez-Villegas, 2006).

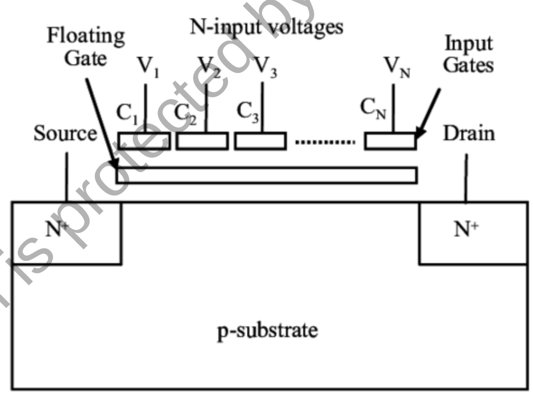

Figure 2.1: Structure of n-type with N-input FGMOS transistor.

(Rodriguez-Villegas, 2006)

2.2.2 Large Signal DC Analysis of FGMOS Transistor

Figure 2.2 illustrates the equivalent schematic and the symbol for an n-type N-input FGMOS (Gupta, 2010).

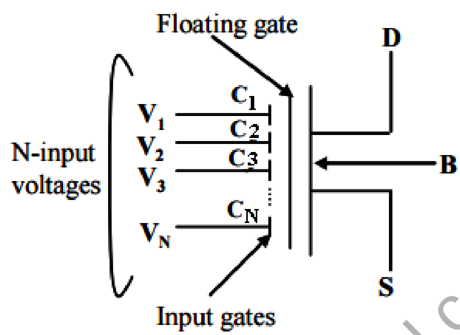

Figure 2.2 (a): Symbol of n-type with N-input FGMOS.

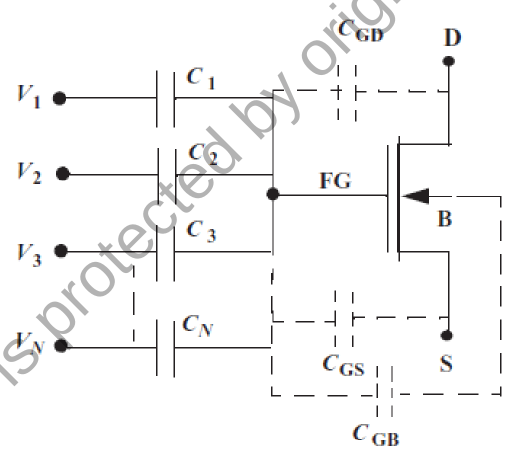

Figure 2.2 (b): Equivalent schematic for an n-type with N-input FGMOS.

Figure 2.2 (a) shows representative for the effective input voltages V_i (for i= 1, 2, …, N) for input (FG), drain (D), source (S) and bulk (B). The sizes of the input electrode are determined by the values of the capacitors that connect the FGMOS inputs to the FG where it can be varied according to the designer's needs given by (2.1) (Rodriguez-Villegas, 2006):

$$C_i = \left(\frac{\varepsilon_{SiO_2}}{t_{SiO_2}} \right) A_i \qquad (2.1)$$

Where ε_{SiO2} = Permittivity of the silicon dioxide.

t_{SiO2} =Thickness of the silicon dioxide between FG and the effective inputs,

A_i = Area of each input capacitor plate.

The relationship between the DC drain to source current and the FG voltage, V_{FG}, of an FGMOS is not affected by parasitic capacitance. C_{GD}, C_{GS} and C_{GB} influence the relationship between V_{FG} and the effective input voltages V_i. In static, the large signal behavior of an FGMOS can be obtained by combining a standard MOS model for the same technology with the equation related as in Figure 2.2 (b). The voltage at the FG is given by the (2.2) by assuming the presence of infinite resistance between the FG and all the surrounding layers and no leakage current between them so that the FG will be perfectly isolated (Rodriguez-Villegas, 2006).

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i + \frac{C_{GS}}{C_T} V_S + \frac{C_{GD}}{C_T} V_D + \frac{Q_{FG}}{C_T}$$

$$= \sum_{i=1}^{N} \frac{C_i}{C_T} V_{iS} + \frac{C_{GD}}{C_T} V_{DS} + \frac{C_{GB}}{C_T} V_{BS} + \frac{Q_{FG}}{C_T} + V_S \qquad (2.2)$$

Where N = Number of effective inputs,

V_S = Voltage of source,

V_D = Voltage of drain,

C_i= Input capacitances linked with effective inputs,

C_T = Total capacitance seen by FG,

Q_{FG} = Amount of charge that has been trapped in the FG.

C_T is the total capacitance seen by FG given by (2.3) (Rodriguez-Villegas, 2006):

$$C_T = C_{GD} + C_{GS} + C_{GB} + \sum_{i=1}^{N} C_i \quad (2.3)$$

Where C_{GD} = Parasitic capacitances of FG with drain,

C_{GS} = Parasitic capacitances of FG with source,

C_{GB} = Parasitic capacitances of FG with bulk.

Input gate (V_1) is used for signal input gate and input gate (V_2) is used for biasing purposes. Considering $V_S = V_B = 0$, V_{fg} is given by,

$$V_{fg} = \frac{C_1}{C_{Total}} V_1 + \frac{C_2}{C_{Total}} V_2 + \frac{C_{fgd}}{C_{Total}} V_{DS} \quad (2.4)$$

By keeping $C_1, C_2 >> C_{GD}$, the drain current (I_D) of the FGMOS when operating in ohmic region is given by (2.5):

$$I_D = \beta \left[\left\{ \left(\frac{C_1}{C_{Total}} V_1 + \frac{C_2}{C_{Total}} V_2 \right) - V_T \right\} - \frac{V_{DS}}{2} \right] V_{DS} \quad (2.5)$$

Where β is tranconductance parameter which is given by (2.6),

$$\beta = \mu_n C_{ox} \frac{W}{L} \quad (2.6)$$

Total FG capacitance, is given by (2.7),

$$C_{Total} = C_1 + C_2 \tag{2.7}$$

As V_T is the threshold voltage. (2.5) may be simplified as (2.8),

$$I_D = \beta\left(\frac{C_1}{C_{Total}}\right)\left[\left(V_1 - V_{T,eff.}\right)V_{DS} - \frac{C_{Total}}{2C_1}V_{DS}{}^2\right] \tag{2.8}$$

Where effective threshold voltage ($V_{t,\,eff.}$) is given by:

$$V_{T,eff.} = V_T + \frac{C_2}{C_1}\left(V_T - V_2\right) \tag{2.9}$$

Thus, the reduction in $V_{T,eff.}$ can be done by selecting $V_2 > V_T$ and $C_2 > C_1$. For saturation region, drain current I_D is given by (2.10) and (2.11) (S. S. Jamuar, 2018),

$$I_D = \frac{\beta}{2}\left(V_{FG} - V_T\right)^2 \tag{2.10}$$

$$I_D = \frac{\beta}{2}\left[\left(\frac{C_1}{C_{Total}}V_1 + \frac{C_2}{C_{Total}}V_2\right) - V_T\right]^2 \tag{2.11}$$

(2.11) can be written as (2.12) and (2.13) (S. S. Jamuar, 2018),

$$I_D = \frac{\beta}{2}k_1{}^2\left[V_1 - \left(\frac{V_T - k_2V_2}{k_1}\right)\right]^2 \tag{2.12}$$

$$I_D = \frac{\beta}{2}k_1{}^2\left[V_1 - V_{Teff.}\right]^2 \tag{2.13}$$

Where, $V_{T,eff.}$ is given by (2.14),

$$V_{Teff.} = \frac{(V_T - V_2 k_2)}{k_1} \tag{2.14}$$

k_1 and k_2 in (2.14) are given by (2.15),

$$k_1 = \frac{C_1}{C_{Total}} \text{ and } k_2 = \frac{C_2}{C_{Total}} \tag{2.15}$$

So, effective threshold can be reduced by changing the bias voltage, (Samir B. Joshi, 2013).

2.2.3 Problems and Solutions of FGMOS Design

There are problems occurs when designing the FGMOS in different nature represents an "error" because initial condition is unknown unless it is somehow fixed. First, it is not a straight forward simulation. Second, an unknown amount of charge might stay trapped at the FG during fabrication process that can cause an unknown initial condition for the FG voltage (Star-Hspice Manual, 2012). Several solutions to the problem are discussed in this literature.

First solution has done by Ramirez-Angulo et al. is based on the simulation model as in Figure 2.3 (J. Ramirez-Angulo, 1997). This model overcomes the simulation problem by connecting a very high value resistor (R_G) between FG node and a set of Voltage Controlled by Voltage Sources (VCVS) that model the addition at the FG described in (2.2). The gains (a_i, a_0 and a'_0) of VCVSs are the ratios between the corresponding input capacitances and the total capacitance seen by the FG as in (2.16) to (2.18). The capacitances are annulled to open circuit at the gate for calculating the DC operating point.