1

LOW VOLTAGE QUASI CLASS-B LINEAR POWER AMPLIFIER FOR WIRELESS COMMUNICATIONS

Jagadheswaran Rajendran, Nitesh Ram Sharma and Harikrishnan Ramiah

1. Introduction

The current trend in data rate increment of wireless communications imposes a great challenge in designing the transmitter system, in particular the Power Amplifier (PA). This is due to the multi-carrier modulation scheme adapted, which is employed in transmitting high data rate information efficiently. A multi-carrier modulation such as OFDMA inherits a disadvantage of high peak to average ratio (PAPR) [1]. High PAPR forces the PA to operate at back off output power from its 1 dB compression point in order to fulfill the stringent linear transmission requirement. This reduces the efficiency of the PA significantly [2]. The solution for this problem can be divided into two categories which are either improving the efficiency of a linear PA or linearize a high efficiency non-linear PA.

The architectures of design preference in efficiency enhancement method are Doherty PA and envelope tracking PA. The Doherty PA, which has two amplifiers connected in parallel, employs the load modulation technique to enhance the efficiency at the back off output power [3]–[6]. A quarter wave transformer is used to modulate the load to improve the efficiency while the IMD3 cancellation is achieved between the main and auxiliary amplifier paving through linearity enhancement [7]. Implementing and integrating a quarter wave transformer on chip will substantially increase the die size

Alternately, a popular method in improving the efficiency of the PA is an envelope tracking, where the supply voltage for the PA is modulated respective to the output power level. This enables the PA to operate at low supply voltage at an equivalently low power level, which in turn boosts up its efficiency. However, the complexity in implementation serves to be the penalty paid. Often, a hybrid chip merger of CMOS solution to modulate the supply voltage and GaAs HBT PA is adapted in the realization of this technique [8].

The reduction in quiescent current delivers a high efficiency PA, however the PA operates close to the cut off point in the I-V curve, which translates to a highly non-linear operation. Conventionally, the feedback and feedforward [9] technique is used to linearize the PA. In current practice, the Analog Pre-Distortion [APD] and Digital Pre-Distortion [DPD] techniques is gaining increasing momentum in the integration. Through these methods, the input signal to the PA is distorted prior to the amplification as such that the magnitude and phase of its non-linear transfer function has an opposite phase and magnitude response from the amplifier. The DPD method highlights the use of DSP processor to generate the non-linear response [10]. Complex integration is the primary disadvantage in DPD. In contrary, APD imparts a simple construction by integrating an additional active device to the input of the power amplifier [11]. A similar cancellation is as well possible with cascode topology integration [12]

In this chapter, the APD technique has been explored to linearize a highly efficient non-linear low voltage PA. The IMD3 cancellation is obtained by designing a driver amplifier, which produces an opposite third order response to the main amplifier's response, thus adding up cancellation at high output power. On the other hand, the biasing current of the main amplifier is optimized by selecting an appropriate conduction angle to produce a low IMD3 component, easing the cancellation process.