Development of Low Power 2.4 GHz Low Noise Amplifier Using Forward Body Bias Technique for Wireless Sensor Network

by

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

AC	Alternating Current
ADC	Anolog to Digital Converter
ADE	Anolog Design Environment
CG	Common Gate
CMOS	Complementary Metal Oxide Semiconductor
CO2	Carbon Dioxide
DC	Direct Current
DRC	Design Rule Check
ERC	Electrical Rule Check
FOM	Figure of Merit
FOM_{RFLP}	Figure of Merit for Low Power Radio Frequency
GSG	Ground-Signal-Ground
IIP3	Third Order Intercept Point
ISM	Industrial, Scientific and Medical
KCL	Kirchhoff's Current Law
LNA	Low Noise Amplifier
LVS	Layout versus Schematic
MIM	Metal Insulator Metal
NF	Noise Figure
NMOS	Negative Metal Oxide Semiconductor
P_{1dB}	1 dB Compression Point
PEX	Parasitic Extraction
PMOS	Positive Metal Oxide Semiconductor

RF	Radio Frequency
SMIC	Semiconductor Manufacturing International Corporation
SNR_i	Signal to Noise Ratio for Input
SNR_O	Signal to Noise Ratio for Output
TSMC	Taiwan Semiconductor Manufacturing Company
ULP	Ultra-Low Power
VCO	Voltage-Controlled Oscillator
VGA	Video Graphics Adapter
WSN	Wireless Sensor Network

LIST OF SYMBOLS

$\emptyset_f$	Semiconductor Parameter
µm	Micrometer
C_F	Feedback Capacitor
Cox	Capacitance per unit gate area
dB	Decibel
dBm	Decibel-milliwatts
GHz	Gigahertz
g_m	Transconductance
g_{mN}	Single Transconductance
g_{mT}	Total Transconductance
mW	Milliwatts
R_F	Feedback Resistor
t_{ox}	The thickness of the oxide layer
V	Voltage (volt)
C	Body-Source Voltage
V_{TH}	Threshold Voltage
V_{TH0}	Threshold Voltage for $V_{BS} = 0$
γ	Process Dependent Parameter
ε_{ox}	The Dielectric
μ_n	Electron Mobility
Ω	Resistance (ohm)

Pembangunan Kuasa Rendah 2.4 GHz Penguat Hingar Yang Rendah Menggunakan Teknik Jasad Pincang Ke Depan Untuk Rangkaian Penderia Tanpa Dawai

ABSTRAK

Rangkaian penderia tanpa dawai (WSN) moden bolehguna telah membawa kepada permintaan pasaran yang besar pada penerima RF kuasa. Untuk beroperasi dengan hanya menggunakan bateri tunggal untuk jangka masa yang panjang secara berterusan, penerima ini memerlukan tahap kecekapan tenaga yang tinggi. Ia juga mencabar untuk mencapai keperluan prestasi sistem untuk WSN yang berkuasa rendah di mana penggunaan kuasa maksimum harus dalam julat lebih rendah dari 1 mW. Oleh itu, objektif projek ini adalah untuk mengkaji, mencadangkan, mereka bentuk dan mengesahkan satu teknik baru untuk kuasa rendah penguat hingar yang rendah (LNA) yang akan diaplikasikan dalam WSN. Satu topologi baru berdasarkan jasad pincang ke depan dengan tatarajah kaskod telah diterima pakai untuk membuat LNA yang sesuai untuk aplikasi kuasa rendah menggunakan CMOS 0.13 μm Silterra teknologi. Terdapat dua reka bentuk yang dicadangkan dalam kerja ini adalah LNA satu peringkat dan LNA dua peringkat. Bagi LNA satu peringkat, voltan bekalan yang rendah sebanyak 0.5 V digunakan untuk mengoptimumkan keseimbangan antara gandaan, angka hingar dan penggunaan kuasa. Keputusan simulasi pasca bentangan menunjukkan bahawa penggunaan kuasa 0.3 mW dicapai dengan 600 μA penggunaan arus yang bertambah baik dengan 62.5 % berbanding dengan kerja sebelumnya. Simulasi kehilangan masukan balik (S11) adalah kurang daripada -18 dB manakala kehilangan keluaran balik (S22) adalah di bawah -15 dB. Selain itu, gandaan (S21) dari 9.86 dB, angka hingar (NF) daripada 5.11 dB dan tertib titik pintasan ketiga (IIP3) daripada -7.5 dBm pada 2.4 GHz diperolehi. Merit angka yang dikira (FOM) daripada 4.62 (1/mW) adalah yang tertinggi di kalangan kerja yang diterbitkan sebelum ini. Bagi LNA dua peringkat, voltan bekalan yang rendah sebanyak 0.55 V digunakan. Keputusan simulasi pasca bentangan menggambarkan bahawa penggunaan kuasa 0.45 mW dicapai dengan jumlah arus keseluruhan ialah 820 μA yang bertambah baik dengan 79 % berbanding dengan kerja sebelumnya. Simulasi kehilangan masukan balik (S11) adalah kurang daripada -17 dB manakala kehilangan keluaran balik (S22) adalah di bawah -12 dB. Selain daripada itu, gandaan (S21) dari 15.1 dB, angka hingar (NF) daripada 5.9 dB dan tertib titik pintasan ketiga (IIP3) daripada -2 dBm pada 2.4 GHz diperolehi. Merit angka yang dikira (FOM) daripada 4.37 (1/mW) adalah yang tertinggi di kalangan kerja yang diterbitkan sebelum ini. Oleh itu, LNA yang dicadangkan adalah sesuai untuk aplikasi WSN.

Development of Low Power 2.4 GHz Low Noise Amplifier Using Forward Body Bias Technique for Wireless Sensor Network

ABSTRACT

The modern disposable wireless sensor network (WSN) markets have put great demands on a low-power RF receiver. As to operate using only a single battery for a long period of time continuously, these receivers require a high level of energy efficiency. It is also challenging to achieve require system performance in such low power WSN where the maximum power consumption should be lower than 1 mW in range. Therefore, the objectives of this project are to study, propose, design and verify a new technique for low power low noise amplifier (LNA) as to be implemented for WSN applications. A new topology based on forward body bias technique with cascode configuration has been adopted to make the LNA suitable for low power applications using CMOS 0.13 µm Silterra technology. There are two proposed design in this work which are single stage LNA and two stages LNA. For a single stage LNA, a low supply voltage of 0.5 V is used to optimize the trade-offs between gain, noise figure and power consumption. The post layout simulation results indicate that the power consumption of 0.3 mW is achieved with 600 µA of current consumption which is improved about 62.5 % compared to the previous work. The simulated input return loss (S11) is less than -18 dB while the output return loss (S22) is below -15 dB. Besides, the gain (S21) of 9.86 dB, the noise figure (NF) of 5.11 dB and the third-order intercept point (IIP3) of -7.5 dBm at 2.4 GHz is obtained. The calculated figure of merit (FOM) of 4.62 (1/mW) is the highest among the previously published work. For a two stages LNA, a low supply voltage of 0.55 V is employed and drawn 820 µA of total current. The post layout simulation results depict that the power consumption of 0.45 mW is achieved which is improved about 79 % compared to the previous work. The simulated input return loss (S11) is less than -17 dB while the output return loss (S22) is below -12 dB. Other than that, the gain (S21) of 15.1 dB, the noise figure (NF) of 5.9 dB and the third-order intercept point (IIP3) of -2 dBm at 2.4 GHz is attained. The calculated figure of merit (FOM) of 4.37 (1/mW) is the highest among the previously published work. Therefore, the proposed LNA is suitable for WSN application.

CHAPTER 1

INTRODUCTION

1.1 Introduction

This chapter presents the background of the research, problem statements of the research, the objectives of the research, follows by the research scopes and then the organization of the thesis.

1.2 Background

A wireless sensor network (WSN) develops very fast in the market because it offers great functions. WSN is a group of low cost, low power, multifunction and small in size of wireless nodes. They work together to collect, process and communicate data wirelessly. WSN is used in many applications such as in remote sensing, monitoring healthcare, security system, home automation and traffic control. While in agriculture, WSN is used to monitor environmental parameters such as temperature, carbon dioxide (CO2) concentration, and humidity, intensity of radiation and wind pressure or speed. The basic specifications of WSN are the reliability, accuracy, flexibility, expenses, the difficulty of development and power consumptions. But the most important specification is power consumption due to the battery powered of the nodes (Bo Zhao and Huazhong Yang, 2010). Consequently, this specification leads to a great development of CMOS RF usage in a research area. The reasons are due to the low cost and size which are capable to be fabricated on a single chip and can be integrated in many applications (Robert Guy Randall, 2008).

The transceiver design related to wireless sensor network applications is classified into three categories: 1) super-heterodyne; 2) low-intermediate frequency (low- IF); and 3) direct conversion. Between these architectures, the direct conversion offers two important consequences which are the reduction of the size and the cost and also lower power consumption. LNA is an irreplaceable block in the front-end of the RF receiver chain (Murad, Ismail, Isa, Ahamd & Han, 2013). The functions of LNA are to amplify the attenuated signal received by the antenna and deliver a significant gain to minimize noise contribution of the subsequent stages, inherently can be handled by the next stages such as mixer and VGA. (Angelos Antonopoulos, Kostas Papathanasiou & Matthias Bucher, 2012).

1.3 Problem Statement

Due to large networks with many nodes of WSN, it is difficult, expensive and impossible for a battery replacement. So, nodes must be able to function ideally up to 10 years, without running out of power (Nathan Michael Pletcher, 2008). LNA is one of the major parts of power contribution in the WSN transceiver (Hafez, Dessouky & Ragai, 2007; Meng Zhang & Zhiqun Li, 2011). In addition, as LNA is the first active device after antenna and because it operates continuously, therefore it is very important to reduce the supply voltage and power consumption for longer usage. Based on the recent published work (Feng Zou, Zhiqun Li & Meng Zhang, 2011), the lowest power consumption obtained is still high which is 2.35 mW. Meanwhile, through low power the gain obtained is not high enough for the LNA specifications to operate which is about 10 dB. Besides, there is a tradeoff between gain and noise figure in choosing a topology for LNA design (Magdy Bayoumi & Saeid Yasami, 2014). The main function of the LNA is, it should provide enough gain in order to overcome noise in the subsequent stage of the receiver. Therefore, the main performance criteria that will be emphasized in designing new LNA circuits is low power consumption but considering other specifications too.

1.4 Research Objectives

The objectives of this research are:

1) To study the various techniques of a low power LNA topology for WSN.
2) To propose and simulate a new circuit design for a low power LNA by using 0.13 μm Silterra CMOS Technology.
3) To design and perform the post-layout simulation of a low power LNA.

1.5 Research Scope

The research is started by exploring the previous topology of a recent low power LNA. The topologies are cascoded and common source cascade for LNA circuit core. While, the forward body bias and self-biased inverter are the LNA of low power topologies. Based on the specifications of a low power LNA, a forward body bias technique with cascode configurations is designed. In order to improve the gain, the second circuit design is proposed with the same topologies but with two stages. After choosing the topology, the circuits are designed using a Composer Schematic Editor in Cadence. Next, the schematics are simulated using the Cadence Spectre anolog design environment as to ensure that the schematic design meets the low power LNA requirements. The layouts are designed after that. The design must pass the Design Rule Check (DRC) and the Layout Versus Schematic (LVS) before performing a post layout simulation. The purpose is to verify the LNA design. Finally, the layouts are optimized as to get the best performances.

1.6 Organisation of the Thesis

This report consists of five chapters. Chapter 1 discusses the overview of the project, problem statement of the project, the objectives of the project, the scopes of the project, and the organization of the report (the report outline).

In Chapter 2, the literature review of the low power LNA is presented. A few topologies of LNA circuit core and LNA low power architectures are discussed in this chapter. Moreover, LNA's performance criteria and a recent progress of CMOS LNA are also presented in this chapter.

Chapter 3 discusses the research methodology of the project. Descriptions of the methodology that are used in software are discussed, including the flowcharts of the project. Then, the specifications of the desired output of LNA are summarized in this chapter. Besides, the proposed schematic and layout of LNAs are discussed in details in the chapter.

Chapter 4 focuses on the simulation results of the proposed LNAs including the gain, input and output matching, noise figure, linearity and also the power consumption that are obtained for the pre layout and also the post layout. The plot of each graph that is presented will be elaborated in this chapter. In addition, the comparison of LNA performance for a single stage as well as two stages between this research and previous works is presented in the chapter.

Chapter 5 concludes all the findings obtained in this research. In this chapter, the discussion of all works is summarized here. The contributions of the research and the plans for further research also are included in this chapter.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Nowadays a low-power RF transceiver becomes a great demand in operating such as in 2.4 GHz Industrial, Scientific and Medical (ISM) bands (Tran Thi Thu Nga, 2012) . This is due to the development of a wireless sensor network (WSN) in recent technology markets. Typically, WSN node is a battery powered. As to ensure that these transceivers can operate with a single battery within one year or more, a high level of energy is required. Therefore, the power consumption of the WSN should be reduced while keeping reasonable receiver sensitivity as to extend a battery lifetime (Zhang Hao, Li Zhiqun, Zhang Meng & Chen Gang, 2010).

In this chapter, a few of previous works for a low noise amplifier design (LNA) will be discussed, but focusing on four techniques of recent topologies which are forward body bias, a self-biased inverter, common source cascade and cascode technique. These architectures are able to minimize power consumption in a typical CMOS for a wireless sensor network (WSN). Besides, performance criterias of the LNAs such as high gain, low noise, input and output matching are also reviewed. As to provide extremely low power and also to optimize all aspects and characteristics, the performance for each topology then is compared. The recent CMOS LNAs are also briefly summarized as a guideline in designing a new low power LNA circuit.

2.2 A Wireless Sensor Network

As a revolutionary technology, Wireless Sensor Networks (WSNs) are well known in providing opportunities in a wide variety of critical applications such as military, home healthcare applications and the environmental science (John A. Stankovic, Anthony D. Wood & Tian He, 2010). As Wireless Sensor Networks require no wires, cables or other infrastructure to start its operation, it becomes easy to deploy. For an operation, current-generation node hardware usually relies on batteries. Therefore, power consumption becomes a critical issue since this energy resource is fundamentally constrained by the small device form factor. Recently, the target is to obtain minimum power consumption, lower than mW (Taeksang Song, Hyoung-Seok Oh & Euisik Yoon, 2006).

As shown in Figure 2.1, LNA is the first active component in the WSN receiver. The function is to amplify an incoming signal. Therefore, it creates a greater demand such as a smaller chip size area, consumes less power, provides enough gain, low noise and high linearity (Thacker, Awakhare, Khobragade & Dwaramwar, 2014). In addition, LNA also needs to provide input impedance matching (T. Sasilathaa & J. Rajab, 2010).

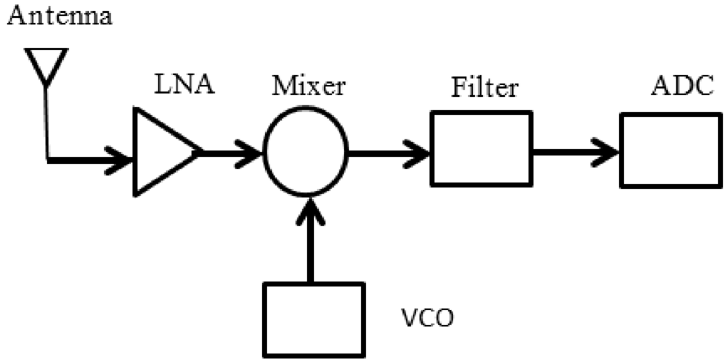

Figure 2.1: A WSN receiver block diagram

2.3 LNA Circuit Core Architectures

2.3.1 Cascode

In designing a LNA, commonly used circuit architecture is cascode. Among the advantages of a cascode design are it can effectively reduce the Miller effect, block the effects of the limited output impedance and offer a good reverse isolation (Eshghabadi et al., 2012; Chong, Ramiah, Tan, Vitee & Kanesan, 2014) (Feng Zou, Zhiqun Li & Meng Zhang, 2011; Hsin-Chia Yang et al., 2013; Shumail, Nisar, Muzaffar, Arshad & Qamar-ul-Wahab, 2013). The improved reverse isolation also provides better circuit stability (Xusheng Tang, Fengyi Huang & Dawei Zhao, 2012). Figure 2.2 shows the typical cascode schematic.

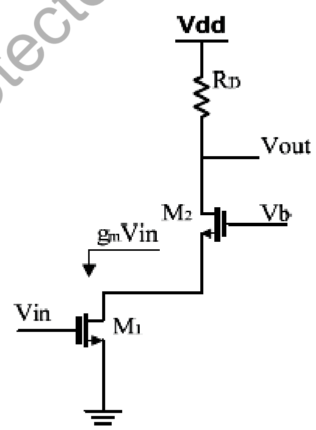

Figure 2.2: The cascode structure (Xusheng Tang, Fengyi Huang & Dawei Zhao, 2012)

Due to the advantages of low noise figure, high gain, good linearity and good input impedance matching, a schematic as shown in Figure 2.3 has been widely employed in the wireless transceiver system (Muhamad, Soin, Ramiah, Noh & Chong, 2013). Since resistive degeneration causes dissipative power loss while affecting the noise figure (Xusheng Tang, Fengyi Huang & Dawei Zhao, 2012), so it is avoided.

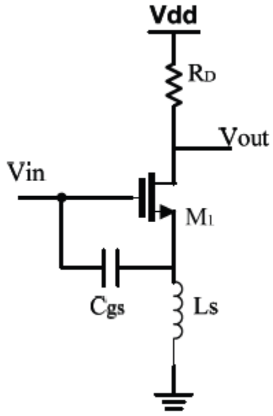

Figure 2.3: Common-source amplifier with negative feedback of source inductance (Xusheng Tang, Fengyi Huang & Dawei Zhao, 2012)

Based on Figure 2.4, the function of transistor M1 and M2 are as input devices. The function of M3 is as a current generator for M4. A better output matching could be attained by varying the bias voltage and also the size of transistor M3 through M4.

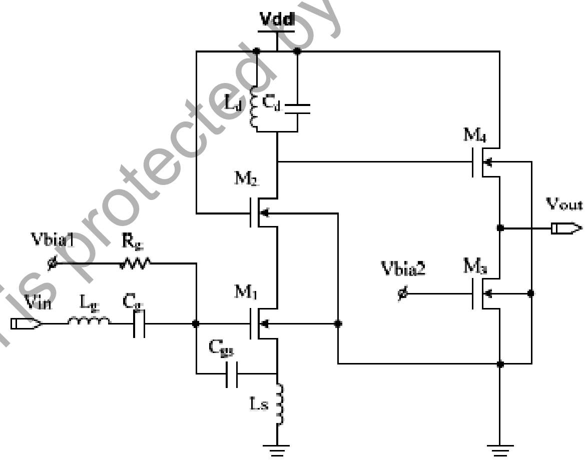

Figure 2.4: The source inductance negative feedback with cascode LNA schematic (Kia, A'ain, Grout & Kamisian, 2013)

Through the source inductance negative feedback with cascode schematic, gain, noise figure and also impedance matching of the LNA can be optimized. Designing SMIC 0.13 μm processes, results in voltage gain is higher than 20 dB while the noise figure is below 1.8 dB. The LNA core operates with 1.2 V supply voltage and the power consumption obtained from this design is 5.8 mW.

2.3.2 Common Source Cascade

A general circuit topology for LNA circuit core is the cascade amplifier. The achievement of high-input impedance and low-noise figure due to the Miller effect makes it suitable for this proposed LNA designed. The LNA circuit topology is shown in Figure 2.5 which contains of two sources follower circuits and a common source cascade amplifier with a passive inductor. The output impedance of the source follower circuit is defined by $1/g_m$ which is equal to 50 Ω.

A feedback resistor R_F in Figure 2.5 is functioning to get 50 Ω input impedance matching. The function of C_F is to avoid overshoot in the frequency response of LNA and for input matching at high frequencies. Transistor M_1 gives an impact to noise figure. By increasing g_{m1}, the power consumption of the first stage will be increased while the noise figure will be decreased (Kia, A'ain, Grout & Kamisian, 2013).

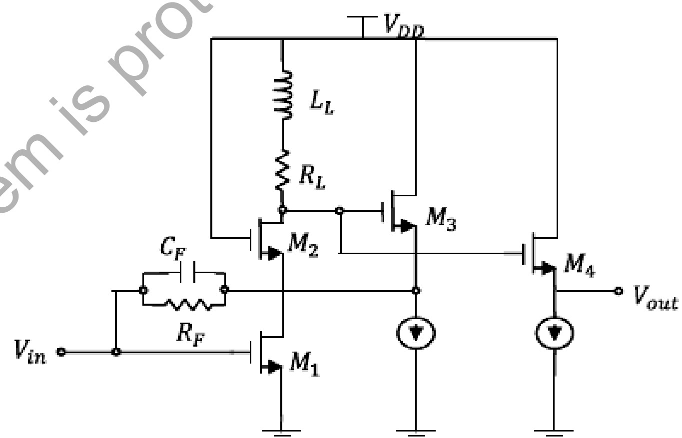

Figure 2.5: The LNA circuit topology (Kia, A'ain, Grout & Kamisian, 2013)

The amplifier circuit has been designed in 0.18 μm CMOS process and is simulated using the Cadence Spectra circuit simulator. The LNA is a common source of cascade amplifier with RC feedback.

2.4 The LNA Low Power Circuit Topologies

2.4.1 The Forward Body Bias

Due to the simplicity of the forward body bias technique; it is used in this topology as to lower down the value of power consumption of the LNA (Wu, Lin & Tsai, 2012) which will be discussed in details as below. This topology of LNA is implemented and designed by using a 0.18 μm CMOS technology. The LNA operates at 2.4 GHz with only 0.6 V of supply voltage and achieves 2.88 dB of NF, 10.1 dB of gain, and power consumption is 0.84 mW. Figure 2.6 shows the schematic of the forward body bias topology.

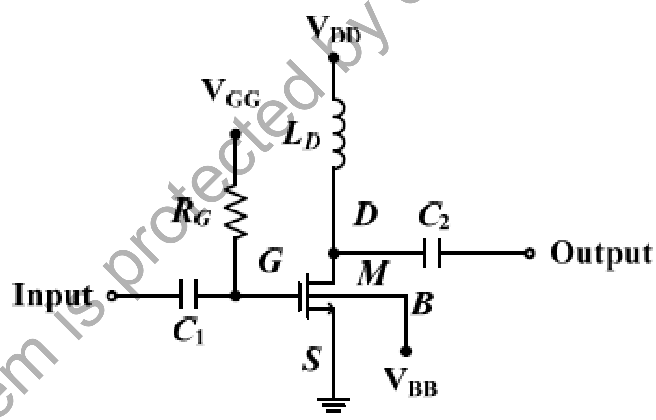

Figure 2.6: The schematic of LNA with a forward body bias technique (Behzad Razavi, 2001)

Typically, the equation between the threshold voltage and the body-source voltage is given as (Dehqan, Kargaran, Mafinezhad & Nabovati, 2012) ;

$$V_{th} = V_{th0} + \gamma(\sqrt{2\phi_f - V_{bs}} - \sqrt{2\phi_f}) \quad (2.1)$$