# CHAPTER 7

# ANALYSIS OF JFET AT LOW FREQUENCY

## 7.1 Introduction

The structure and characteristics of JFET have been discussed at length in Chapter 5. This chapter is aimed at the derivation of its low frequency model and analysis of its properties when biased as an amplifier.

Among the advantages of FET devices is its application in low frequency or small signal amplifiers which are capable of giving large voltage gain at very large input resistances. The best configuration for this application is the common source amplifiers where input signal is applied at the gate and output is taken from the drain, and source is common for both input and output. The common drain configuration results in gain which is almost unity while the common gate configuration is seldom used even though it gives voltage gain without changing the polarity.

## 7.2 JFET Small Signal Model

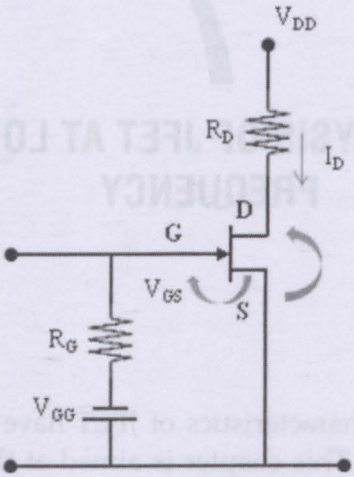


**Figure 7.1: A Common Source JFET Amplifier.**

The analysis of a JFET amplifier at low frequency needs a small signal model which represents the behavior of the FET transistor. Consider an amplifier circuit in Figure 7.1 where a JFET transistor is connected in common source configuration. Voltage source $V_{DD}$ and $V_{GS}$ gives the correct biasing current and voltage such that the amplifier operates at the pinch off region. Recalling the output characteristics of JFET amplifier in Chapter 5, the output current, that is the drain current, $I_D$ depends on both the output voltage $V_{DS}$ and input voltage $V_{GS}$.

Therefore, $V_{DS}$ and $V_{GS}$ are chosen as independent variable. Observe that unlike in the bipolar transistor case, there is only one variable depending on this independent variable and that is $I_D$. The other variable, $I_G$ which is also the input current is always zero since the gate is reversing biased.