Development of RTL Platform Validation Methodology for Customized Wireless Microcontroller Unit

by

Nurul Zhafirah Binti Muhammad
(1630312304)

A thesis submitted in fulfillment of the requirements for the degree of
Master of Science in Electronic Engineering

Faculty of Electronic Engineering Technology
UNIVERSITI MALAYSIA PERLIS

2021

ACKNOWLEDGEMENT

All praises to the Great and Merciful Allah and his blessing for the completion of this thesis. I am grateful for all the opportunities, trials and strength that have been showered on me to complete the thesis.

First and foremost, I would like to express my upmost sincere gratitude to my supervisor Ir. Dr. Azizi Harun for his continuously support, motivation and patience for me to complete my master research with valuable results. All his endeavors have been very much appreciated.

My deepest gratitude to my beautiful and precious family for the continuous support. It would not have been possible for me to finish writing this thesis without their support. I would like to thank my Umi Pn. Jizah and my Abah En. Muhammad, my siblings Kak Ayu, Abang Aiman, Angah and my younger brother Akhir for their enormous support and love.

To all my friends, thank you for listening, offering me advice, supporting me through this and for all the memories we have for entire process. May this friendship will last until the end.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

IoT	Internet of things
IC	Integrated circuit
SoC	System on chip
MCU	Microcontroller unit
3D	Demand driven development
RTL	Register transfer level
TDSP	Temperature digital signal processing
SRAM	Static random-access memory
BTLE	Bluetooth low energy
RTC	Real time clock
SPI	Serial peripheral interface

LIST OF SYMBOLS

∑	Summation of statements line
%	Percentage

Pembangunan Metodologi Pengesahan RTL Yang Disuaikan Untuk Unit Mikrokontroler Tanpa Wayar

ABSTRAK

Permintaan untuk unit mikrokontroler tanpa wayar telah berkembang kerana keperluan bagi penyelesaian perkara internet hujung-ke-hujung, keperluan produk, dan potensi harta intelek yang dicipta. Oleh yang demikian, pembangunan reka bentuk yang rumit dicipta disebabkan oleh revolusi teknologi sistem yang dibenamkan di dalam satu cip, menyebabkan masalah masa yang dihabiskan di bidang pengesahan meningkat untuk sesuatu reka bentuk baru yang dibangunkan. Oleh itu, penyelidikan ini diketengahkan pada metodologi Pengesahan RTL dengan menggunakan kaedah yang sedia ada untuk mikrokontroler yang baru dicipta bagi mengatasi masa yang dihabiskan untuk pengesahan tersebut. Sebagai tujuan penyelidikan ini untuk mencari kaedah terpantas yang dapat disesuaikan dengan reka bentuk mikrokontroler semasa, maka pengesahan RTL ini dibahagikan kepada dua tahap iaitu tahap modul dan tahap sistem. Untuk tahap modul, pengesahan difokuskan pada sumber kod harta intelek. Oleh itu, di peringkat modul ini, metode berdasarkan simulasi, yang merupakan teknik liputan kod telah digunakan dan dilaksanakan dalam lingkungan kotak putih untuk mengesahkan kualiti kod dan untuk mendapatkan liputan maksimum yang wajar untuk diperolehi. Untuk sistem MCU ini, liputan munasabah yang perlu diperoleh pada tahap modul adalah lebih daripada 80%. Kelebihan teknik liputan kod adalah kesalahan reka bentuk dapat dikesan pada tahap awal. Sekiranya IP hanya mencapai liputan yang disasarkan maka akan beralih ke tahap pengesahan berikutnya, iaitu tahap sistem. Jika tidak, reka bentuk harta intelek ini dinyatakan tidak berjaya dan perlu untuk menghasilkan reka bentuk semula seperti yang ditetapkan. Sementara itu, untuk tingkat sistem, verifikasi dilakukan berdasarkan pelaksanaan bangku uji untuk mengesahkan sistem dengan satu set vektor ujian. Maklumat terperinci mengenai teknik yang digunakan dan hasil penyelidikan ini disajikan dalam tesis.

Development of RTL Platform Validation Methodology for Customized Wireless Microcontroller Unit

ABSTRACT

Demand for customized wireless microcontroller unit (MCU) has been expanding due to the requirement of end-to-end IoT solution, product requirement, and potential IP. As such, the development for design complexity growth poses by the evolution of the SoC technology, causing the issue of time spent in the area of validation has increasing for the newly complex design developed. Thus, this research was highlighted on the RTL Platform Validation methodology by utilizing the existing method for newly developed MCU to overcome the time spent on the validation. As the goal of this research to find the fastest method that can be customized to the current MCU design, hence this RTL validation were divided into two levels which were module level and system level. For module level, the verification was focused on the IP's source code. Thus, in this module level, the simulation-based method, which is code coverage technique was utilized and being implemented in white box environment as to verified the quality of the codes and to obtain the maximum reasonable coverage to be covered. For this MCU system, the reasonable coverage that needs to be obtained at the module level was more than 80%. The advantage of the code coverage technique was the bugs and errors of the design can be detected at the early stage. As if the IP only achieves the targeted coverage than will move to the next level of verification, which is system level. Otherwise, the IP design was declared as unsuccessful and resulting to redesign as specified. Meanwhile, for system level, the verification was based on the implementation of test bench as to verify the system with a set of test vector. The detailed on the techniques used and the results of this research were presented in the thesis.

CHAPTER 1 : INTRODUCTION

1.1 Research background

The introduction of the internet of things (IoT) on the global level has led to the emergence of the uses of wireless devices. The main purpose of these IoT things is to help people live and work smarter with the help of smart technologies for everyday life (Coulby et al., 2020). This internet of things (IoT) paradigm has become a phenomenon in the electronic field inadvertently increased the number of devices by end-users (Standards.ieee.org, 2018). The expectation to see the same users with a new generation of IoT devices has led towards higher complexity of integrated circuit (IC) supporting System on Chip (SoC). Advancement of the complexity design in IC has drawn attention to the uses of a microcontroller unit (MCU) for IoT. Meanwhile, the demands from the clients to have a sophisticated electronic system in a single chip make the MCU a great choice of hardware for its applications (Barnasconi et al., 2015 and Schwierz et al., 2016) by improving the efficiency and the operation of the MCU. By looking towards the current technology situation in the IC design industries, the idea to have the first MCU made in Malaysia has been a realization in one collaboration program called 3D (Demand Driven Development) Program. This program was the collaboration between local universities and the well-known electronic companies as Intel, Altera, Oppstar, MiCDA, and Silterra under the supervision and sponsored by Talent Corp Malaysia under the Industry-Academia Collaboration (IAC) for Sector. The most important outcome for this program was the network of universities capable of producing IP(s) that builds IC designers in universities that creates the funnel of industry-ready graduates for the IC Design cluster.

The wireless MCU was developed by referring to the Nordic Semiconductor “Nrf51822 Multiprotocol Bluetooth® low energy/2.4 GHz RF System” as the benchmark in its design. This product was chosen as the benchmark product for this project because of its capability whereas the digital and analog system was on one single chip. Hence, the design of the block diagram for this wireless MCU as in Figure 1.1. The figure shows the MCU was designed based on the AMBA bus integrated with the feature IPs such as ADC/DAC, PLL, RTC, BTLE controller, AES, Temperature Sensor (TDSP) and SPI and basic IPs such as JTAG, MCU, RAM, ROM, CLOCK and Power management. This MCU was newly developed without the knowledge of its internal workings but only shows the interconnections between the various IPs and communication protocols (Schwierz et al., 2017) Same standard as development for other IC design, this wireless MCU also need to pass the test of RTL Integration, RTL Validation, Full chip verification and Full chip Integration DFT before release the product to the customer (Rawat et al., 2020 & Villarroel, 2019).

Despite of that, this thesis highlights on the RTL Validation of the wireless MCU for the feature and basic digital IPs such as SRAM, TDSP, RTC, SPI and BTLE. RTL Validation was an important part in the development as in every IC design needs to come out with the new RTL Validation platform for customized the current designs. This is because of not every existed method was compatible to the new design. As this MCU was design without the knowledge of its internal workings, hence the involved IPs designed would follow as Nordic Semiconductor requirement and being validated by that specification. The goal of this research was to support RTL platform validation for a newly developed and customized MCU and provide the method that could be use to overcome or reduce the bottleneck of the current validation issue even for other newly IC developed. Thus, the study and research on the RTL validation has been done and described in this thesis. In the literature study shows the more sophisticated of the system, increased the sizes of the designs. As the sizes of the design increase, the efficient usage of validation methodologies would have a strong impact on verification productivity and faster time to market. The complexity of the designs causes the difficulty in the RTL validation to allow the bottleneck to be seen at the infancy in the design cycle and produces quality IC (Standards.ieee.org, 2018). Such spontaneous increased in complexity design poses unequivocal complicated Register Transfer Level (RTL) validation strategies.

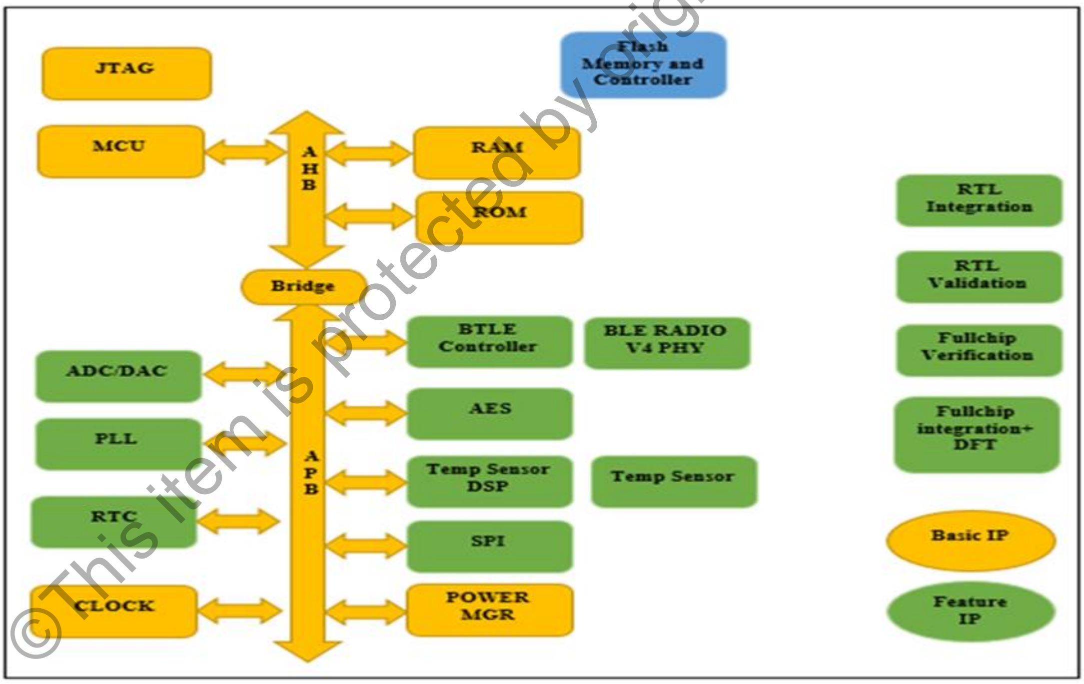


Figure 1.1 : Wireless Microcontroller (MCU)

1.2 Problem statement

As the demand for development-driven initiative increases, more development on the driven such as a microcontroller unit (MCU) has been developed to meet the requirement. Advertently, the need for customized wireless microcontroller unit (MCU) has been expanding due to the requirement of end-to-end IoT solution, product requirement and potential IP. As with other RTL design and development, this design and development also require RTL platform validation to ensure the successes of integration.

However, the validation issues make it arduous for engineers to achieve the validates. The explicit problem in this issue is the design complexity growth poses by the evolution of the SoC technology. This is proven by the study of the trends in functional verification (Foster, 2015) as it shows the electronic industry continues to move to a larger design. Figure 1.2. shows the trends from 2007, 2012, and 2014 studies in terms of the logic gate. As in the graph, the size of the logic gate keep increase in the design since 2007 until 2014. In the year 2007, the highest logic gate achieved in the design was only less than 40M gates but shows the increase in the year 2012 by 80M and up to over 500M logic gate size of the design in the year 2014 proved that the electronic industry has moved to large design year by year.

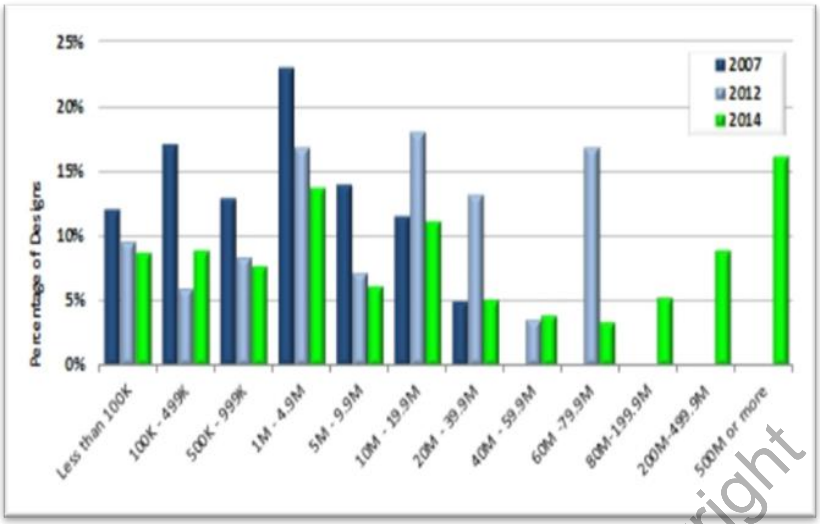
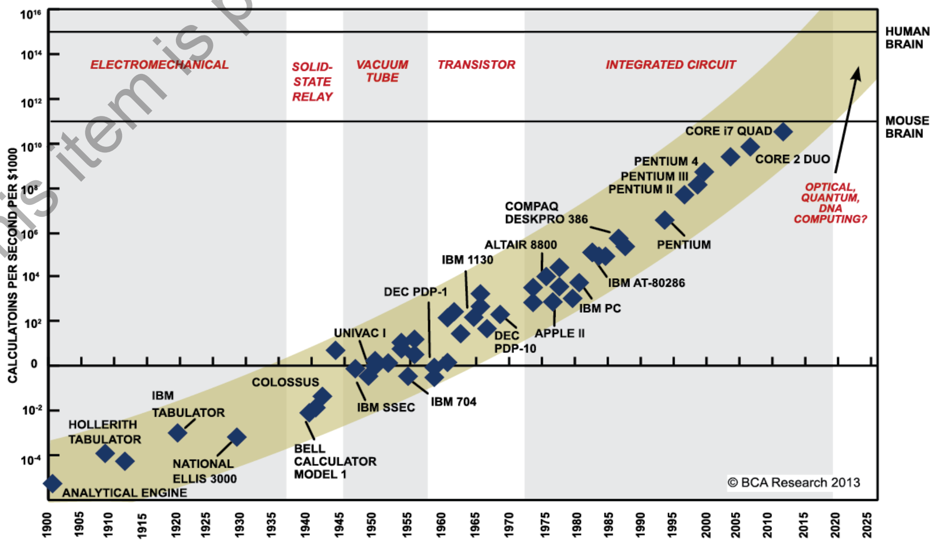


Figure 1.2 : Trend of Electronic Study

The advancement of the design size happens as expected as shown in the study of the Moore law. As demonstrated in Figure 1.3 that the number of transistors on microchip doubled for every two years as well as the performance of the chip.



SOURCE: RAY KURZWEIL, "THE SINGULARITY IS NEAR: WHEN HUMANS TRANSCEND BIOLOGY", P.67, *THE VIKING PRESS*, 2006. DATAPOINTS BETWEEN 2000 AND 2012 REPRESENT BCA ESTIMATES.

Figure 1.3 : Moore’s Law Concept (Muhammad et al., 2017)

The increment in the design sizes is only one of the aspect in the growth of the sophisticated technology (SoC evolution).This evaluation of SoC design which includes the control processor, mix signal digital and analog and complex bus architecture (Foster, 2015) give a big challenging to the verification process especially using the traditional method. Other considered problem is time spent on the verification exceeds the time spent on the design.

Figure 1.4 presented the condition regarding the matter. According to the (Molina & Cadenas, 2007) the statistic reported that 60-70% of the entire product cycle for a complex logic chip is spent to verification part.

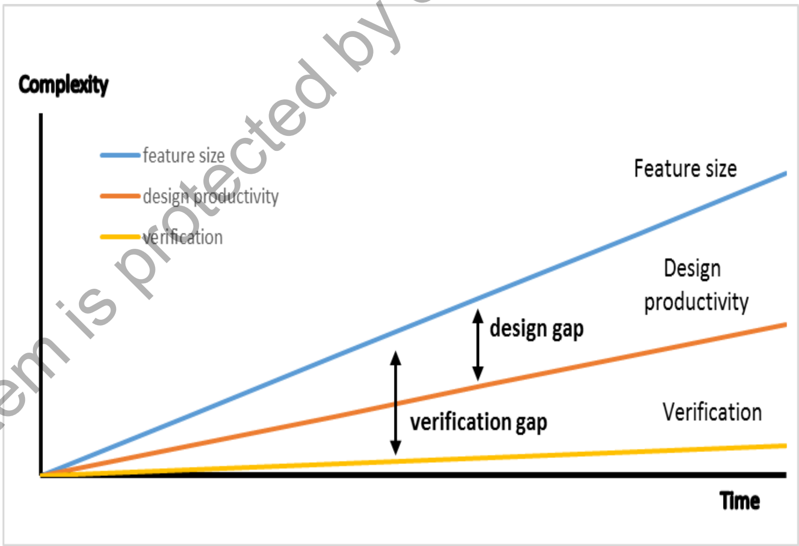


Figure 1.4 : The Gap of Design Complexity versus Time

Thus, this research allows the exposure of different methods as reported in the literature to overcome the validation issues and find the most suitable method to fit the current design and limited time given by utilizing the existing method.

1.3 Research objective

The main purpose of the research is to support RTL platform validation for a newly developed and customized MCU. As such, this research is meant to serve the following objectives:

a) The foremost objective is to analyse existing methodology for RTL platform validation on a newly developed customized wireless microcontroller unit (MCU).

b) To develop validation methodology based on reusable techniques.

c) To execute validation methodology on a wireless microcontroller to achieve reasonable coverage.

1.4 Research scope

In this research, the goal of platform validation or known also as functional verification was to ensure the logic design of the IPs conformed to the specification. Functional verification was literally divided into two methods, simulation-based and formal verification. Moreover, the RTL validation was carried out at two levels, which were unit level and chip level. Hence, this research limited to the study on simulation-based technique and formal verification to be applied on the RTL validation platform for the five digital unit levels of the newly developed MCU which were SRAM, TDSP, RTC, SPI, and BTLE. The comparison between these two functional verification techniques as described in this thesis. In addition, this research will be covered on the code execution and presented the percentage of coverage area that has been covered for newly developed MCU.

1.5 Expected outcome

The imperative outcome in this research was to verify the design of IPs was correctly follow the requirement and the code was executable and able to achieve the reasonable percentage coverage depends on the technique used as the quality of the design was measured by that (Gergely et al., 2019 and Tengeri et al, 2015)). Based on the testing technology, the reasonable coverage for the system with most coverage metrics was 70-80% (Cornett, 2013 and Prause et al., 2017). However, the coverage percentage was negotiable based on the system developed but importantly able to cover in every functional and non-functional area of the design source code.

1.6 Thesis organization

The thesis is organized like in Chapter 1, summarizing on the research background and upbringing the issues of the research and the main goal to overcome the things. Chapter 2 presented the existing methods of RTL platform and the comparison for the techniques to be applied on this verification as if these methods were still competent to the current design. Meanwhile, the essential steps on the verification were described and the description of the coverage percentage to be calculated was presented in Chapter 3. In chapter 4, the verification results of each of five digital IPs, SRAM, TDSP, RTC, SPI, and BTLE were presented and discussed. Finally, the conclusion and future work that foresees to be continued in the research was stated and discussed in Chapter 5.

CHAPTER 2 : LITERATURE REVIEW

2.1 Introduction

This chapter presented the literature review of associated methodology in RTL validation for the wireless microcontroller. As discussed in the previous chapter, the major issues of the RTL Validation were the designs getting larger and complex. Therefore, this chapter discussed in detail the advantages and disadvantages of the existed methods implemented in the current designs. In addition, various techniques have been explored in this research to customize the wireless microcontroller.

2.2 Verification complexity

The integrated circuit had gone through the revolution in the last couple of decades aligned with the law that shows remarkably precise indicator of chip complexity for the VLSI era (Mollick, 2006; the evolution of the digital circuit design, 2000). In the year of 1965, a famous physical chemist who co-founded Intel Corporation, Gordon E. Moore in his paper for Electronics magazine's 35th anniversary had established the state of "number of transistors in a dense IC doubles approximately every two years" (Mollick, 2006). His well-known statement is defined as Moore's Law and been credited with being the engine of the electronic revolution (Mollick, 2006). With the success of being an accurate indicator for chip complexity in VLSI in the late 1970s, Moore's law had proven to be accepted as a dependable guide for the future revolution in electronic designs (Mollick, 2006).