EFFECT OF NICKEL MICROALLOYING ON THE MICROSTRUCTURE AND PROPERTIES OF In-35 wt%Sn LOW TEMPERATURE SOLDER

by

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

3D IC	Three-dimensional integrated circuit
Ag	Argentum
Al_2O_3	Alumina
Al	Aluminum
Au	Gold
Bi	Bismuth
BGA	Ball grid array
BSE	Backscattered electron
BN	Boron nitride
Cu	Copper
OSP	Organic solderability preservative
CTE	Coefficient thermal expansion
DSC	Differential scanning calorimeter
EDX	Energy dispersive X-ray spectroscopy
EU	European Union
FCBGA	Flip chip ball grid array
FO-WLP	Fan-Out Wafer-Level Package
HSS	High speed shear
HVTEM	High voltage transmission electron microscope
In	Indium
In_2O_3	Indium Oxide
IMC	Intermetallic compound
LTS	Low temperature solder
µ-bump	Micro-bump
µ-XRF	Micro-x-ray fluorescence
Ni	Nickel
OM	Optical Microscope
P	Phosphorus
Pb	Lead
PCB	Printed circuit board
PDF	Powder diffraction file
PBGA	Plastic ball grid array
PoP	Package on package

RT	Room temperature
RMA	Rosin mildly activated
RoHS	Restriction of Hazardous Substances
SAC	Tin-Argentum-Copper
SAED	Selected area electron diffraction
Sb	Antimony
SEM	Scanning electron microscope
Si	Silicon
SiC	Silicon carbide
SiP	System in package
Sn	Tin
SXRI	Synchrotron X-ray radiography imaging
Te	Tellurium
TEM	Transmission electron microscope
Ti	Titanium
TM	Tabletop microscope
TSV	Through-silicon-via
UTS	Ultimate tensile strength
WEEE	Waste Electrical and Electronic Equipment
XRD	X-ray diffraction
XRF	X-ray fluorescence
YS	Yield strength
Zn	Zinc

LIST OF SYMBOLS

wt%	Weight percent
°C	Degrees Celcius
K	Kelvin
mA	Milliampere
μΩ	Microohm
cm	Centimeter
mm	Millimeter
μm	Micrometer
nm	Nanometer
h	Hour
min	Minutes
s	Second
g	Gram
°	Degree
f_S	Faction solid
T	Tesla
ΔT	Degree of undercooling
ΔT_n	Nucleation undercooling
ΔT_{max}	Maximum undercooling
T_g	Glass transition temperature
T_n	Cooling curve onset temperature
T_m	Heating curve peak temperature
T_{re}	Cooling curve peak
T_C	Critical temperature
B_C	Critical field
J_C	Critical currents density
θ	Theta
H	Hour
N	Newton
Å	Armstrong

Kesan Pengaloian Micro Nikel ke atas Mikrostruktur dan Sifat-sifat Pateri Suhu Rendah In-35 wt%Sn

ABSTRAK

Seiring dengan industri mikroelektronik yang menghadapi cabaran dalam mengikuti Hukum Moore tetapi dihadkan oleh pengkecilan saiz komponen, prestasi aloi pematerian dalam pemasangan elektronik menjadi penting. Penggunaan bahan pematerian aloi bebas plumbum (Pb) telah menimbulkan isu berkaitan dengan suhu pemprosesan yang lebih tinggi menyebabkan lengkungan dinamik, prestasi berkurangan, dan keraguan mengenai daya kekuatan penyambungan. Bagi meningkatkan prestasi process pematerian, tesis ini menyelidik penggunaan bahan pematerian aloi suhu rendah (LTS) In-35Sn (wt%) dengan penambahan 0.05 wt% nikel (Ni). Penyelidikan ini menggunakan kaedah ujian seperti pengimejan synchrotron X-ray radiografi secara masa nyata (SXRI), mikroskop imbasan elektron (SEM), mikroskop imbasan elektron pemindahan (TEM), kalometri pengimbasan perbezaan (DSC), dan ujian ricih berkelajuan tinggi (HSS) untuk menganalisis mikrostruktur aloi pateri dan prestasi penyambungan. Permerhatian SXRI masa nyata mendapati interaksi kompleks berlaku semasa pemejalan aloi dan Ni memberi impak kepada perubahan mikrostruktur termasuk pengurangan pertumbuhan dendrit primer dan jarak antara sekunder sebanyak faktor 0.652 dan 0.502. Interaksi ini sukar diperhati menggunakan kaedah konvensional yang menyediakan mikrograf mikrostruktur pepejal. Selain itu, tesis ini meneroka perubahan mikrostruktur semasa pembentukan sebatian antara-logam $Cu_3(Sn,In)$ (intermetallic compound, IMC) dan pemejalan aloi pateri In-35Sn pada substrat kuprum (Cu). Pemerhatian SXRI mendapati Ni memberi titik nukleasi untuk penumbuhan β-In_3Sn dan meningkatkan suhu untuk pemejalan pateri aloi. Tambahan pula, TEM analisa mendapati Ni terdapat dalam $Cu_3(Sn,In)$ dan menghasilkan mikrostruktur yang lebih halus, serta meningkatkan sifat mekanikal semasa ujian HSS dengan peningkatan sebanyak 5.62% dan 3.45%, dan tenaga permulaan patahan sebanyak 4.35% dan 18.55% semasa ujian pada kelajuan 100 mm/s dan 2000 mm/s. Seterusnya, tesis ini mengkaji kesan proses kitaran haba berganda semasa proses pemasangan pakej elektronik terhadap pertumbuhan partikel $Cu(Sn,In)_2$, lapisan $Cu_3(Sn,In)$, serta kesannya terhadap sifat mekanikal. Hasil kajian ini medapati penambahan mikroaloi Ni memberi perubahan nukleasi dan pengurangan kinetik pertumbuhan partikel $Cu(Sn,In)_2$ sebanyak 60% dan meningkatkan penyerapan tenaga ricihan sebanyak 20.77%, 35.40%, dan 6.85% semasa kitaran haba yang pertama, ketiga, dan keenam. Secara keseluruhannya, hasil penyelidikan ini menunjukkan bahawa penambahan Ni memberi kesan terhadap pemejalan aloi, tindak balas antara permukaan aloi pematerian dan Cu, dan pembentukan fasa. Pendekatan ini secara berkesan mengubah mikrostruktur dan meningkatkan prestasi pematerian aloi In-35Sn pada substrat Cu. Hasil penyelidikan ini memberi permahaman yang mendalam tentang kelakuan aloi dan memberikan kesan secara praktikal untuk inovasi komposisi LTS baharu. Kajian ini akan menyumbang kepada kemajuan pembungkusan mikroelektronik dengan mengkaitkan pemahaman saintifik dengan kebolehgunaan industri bagi mendorong perkembangan dalam penggunaan aloi pematerian suhu rendah yang lebih baik dalam pembangunan domain penyusunan elektronik bebas Pb.

Effect of Nickel Microalloying on the Microstructure and Properties of In-35 wt%Sn Low Temperature Solder

ABSTRACT

As the microelectronics industry faces challenges in sustaining Moore's Law due to physical limitations in component miniaturization, the reliability and performance of solder joints in electronic assemblies becomes crucial. The adoption of lead-free solder materials has raised concerns related to processing temperatures inducing dynamic warpage, reduced yield, and reliability concerns. To address these challenges, this thesis investigates the use of low temperature solder (LTS), specifically In-35Sn (wt%) solder with 0.05 wt% nickel (Ni) microalloying. Various techniques, including synchrotron X-ray radiography imaging (SXRI), scanning electron microscope (SEM), transmission electron microscope (TEM), differential scanning calorimeter (DSC), and high-speed shear (HSS) testing are employed to comprehensively analyze the prepared solder, microstructure and soldering behavior. In-situ real-time SXRI observations reveal complex interactions during the solidification of the alloy, providing insights into how Ni suppresses primary arm growth by a factor of 0.652 and reduces secondary arm spacing by a factor of 0.502, impacting microstructure evolution. These interactions are challenging to observe using conventional methods that provide micrographs of solidified microstructures. Furthermore, the thesis explores microstructure evolution during solidification and the formation of interfacial $Cu_3(Sn,In)$ intermetallic compounds (IMCs) in In-35Sn solder alloys on copper (Cu) substrates. The SXRI observations reveal Ni microalloying providing nucleation sites for the β-In_3Sn phase and reducing the degree of undercooling to near zero. Additionally, the TEM observations reveal that Ni microalloying results in refining microstructures of interfacial IMCs formation in In-35Sn solder on Cu substrates, and improving mechanical properties by increasing shear strength by 5.62% and 3.45%, respectively, and increasing fracture initiation energy by 4.35% and 18.55%, compared to the reference solder joint during shear at speeds of 100 mm/s and 2000 mm/s. Furthermore, the thesis investigates how multiple reflow cycles during assembly processes impact primary $Cu_2(In,Sn)$ particles, the interfacial $Cu_3(Sn,In)$ layer, and solder joint shear strength. The findings validate nucleation and solidification kinetics and demonstrate a 60 % refinement of $Cu_2(In,Sn)$ particles and increased energy absorption of the solder joint by 20.77%, 35.40%, and 6.85% during the first, third, and sixth reflows. Collectively, the results show that Ni microalloying profoundly impacts alloy solidification, interfacial reactions, and phase formation. This approach effectively modifies microstructure and enhances the properties of In-35Sn solder joints on Cu substrates. The findings not only deepen the understanding of alloy behavior but also offer practical implications for the design of novel LTS compositions. This work contributes to the advancement of microelectronics packaging, bridging the gap between scientific understanding and industrial applicability, paving the way for improved and reliable LTS joint solutions in the development of Pb-free electronics assembly.

CHAPTER 1 : INTRODUCTION

1.1 Research background

In the development of advanced electronic packaging, the pursuit of device miniaturization, improved performance, and enhanced functionality had made high-density packaging technologies essential. These technologies aim to reduce joint sizes while simultaneously improving the properties of packaging materials, ultimately increasing the speed and performance of electronic devices. The demand for reduced device size and enabling the creation of complete conducting circuits in electronic interconnection for large-scale production have highlighted the increasing importance of solder bumps technology for solder joints in electronic assemblies. Solder is a fusible metal alloy with a relatively low melting temperatures, provides the necessary ductility to connect metals. Solder joint not only provides electrical contacts but also mechanical support in electronic assemblies by physically holding components together, accommodating thermal expansion and contraction, heat dissipation, and signal transmission. To achieve higher packaging density and efficient space utilization involves the integration of multiple stacked boards, requiring multiple reflow processes (Chen, Chiu, Chiu, Lee, & Lin, 2017; Zhang et al., 2022). Navigating the challenges posed by size constraints and the complexity of electronic assembly, including stacked Package-on-Package and System-in-Package configurations, makes multiple reflows processes necessary to address reliability concerns associated with the trend towards finer pitch and smaller size.

Traditionally, tin-lead (Sn-Pb) solder with a eutectic temperature of 183 °C is considered as an ideal for many decades. Yet, the use of lead (Pb) has been restricted

since 1st July 2006, by the Waste Electrical and Electronic Equipment Directive (WEEE) and the European Union Restriction of Hazardous Substances Directive (RoHS) (Zhong, Zhang, Li, Long, & Wang, 2022). These regulations have stimulated extensive research into Pb-free alternatives, such as Sn-Cu, Sn-Ag, and Sn-Ag-Cu, as substitutes for Pb-based solders. Nonetheless, these Pb-free alternatives often feature higher melting points compared to the ubiquitous Sn-Pb solder (Cheng, Huang, & Pecht, 2017).

In response to these challenges, research into low temperature solder (LTS) alloys has gained prominence in the microelectronics industry, particularly for electronic packaging. The demand for Pb-free LTS arises from the need to protect temperature-sensitive electronic devices from damage caused by high operating temperatures. Additionally, the evolving landscape of electronics anticipates the emergence of flexible, bendable, and wearable devices. To cater to the need of these flexible electronics, the development of novel LTS In-Sn solder is essential to avoid thermal damage to components and ensure compatibility with manufacturing processes. Notably, In-Sn alloys are known for their high ductility and extended fatigue life, making them ideal for applications in flexible, stretchable, bendable, and wearable electronic packaging technology (Liu, & Tu, 2020; Wang, Mao, Shi, Zhang, & Zhang, 2019; Xu et al., 2020; Zhou, Tan, McDonald, & Nogita, 2022). Furthermore, In-Sn alloys have been identified as potential superconducting solder. Among a series of In-Sn solder, In-35Sn (wt%) has emerged as the most promising, with a melting temperature of 125.5 °C (Zhou, Tan, Gu, McDonald, & Nogita, 2023). This is primarily due to its highest superconducting properties, primarily attributed to its high fraction of β-In_3Sn superconducting phase (Santra et al., 2019).

1.2 Problem statement

The transition from Sn-37Pb solder to lead (Pb)-free alternatives has been driven by environmental concerns and regulatory measures, making Pb-free solder alloys a focus of extensive research and development. Common Pb-free solder alloys, such as SAC (Sn-Ag-Cu) and Sn-Ag, have higher melting points above 217 °C, posing challenges in electronic assemblies due to coefficient of thermal expansion (CTE) mismatches, dynamic warpage, and defects like solder bridging and open joints. In response to these challenges, low-temperature solder (LTS) alloys have gained prominence for addressing these challenges in delicate electronic substrates. Additionally, the advantageous manufacturing characteristics of low-temperature soldering reduce energy consumption, aligning with the electronics industry's growing focus on energy efficiency and sustainability. In response to this, the In-Sn solder alloy has emerged as a promising alternative due to its inherent softness, ductility and fatigue resistance (Liu et al., 2020; Xu et al., 2020). Conventional ex-situ microstructure examination techniques, through widely employed are unable to provide comprehensive insights into the intricate solidification process during reflow soldering on substrates, which influenced by factors such as environmental conditions and microalloying additions. Hence, there is a need to explore more effective methodologies to deepen the understanding of dynamic processes and microstructure evolution during solidification. In-situ synchrotron X-ray radiography imaging emerges as essential for real-time visualization of microstructure evolution and defect formation during solidification. This approach is essential for comprehending the effects of Ni microalloying on the development of In-35Sn LTS microstructure.

Furthermore, solder bump technology plays a vital role in space utilization and high-density devices, making the proportion of intermetallic compounds (IMCs) in these

solder bumps increasingly important. Effective control over IMC growth is crucial for ensuring the reliability of solder joints. Thus, there is a continuous effort to enhance Pb-free solder alloys involves the microalloying technique. Microalloying involves the introduction of trace amounts of additional elements into the alloy composition, leading to a significant modification of the microstructure through the redistribution of the composition or the introduction of an additional new phase in the solder alloys during solidification (Zeng et al., 2015). In this context, the microalloying addition of 0.05 wt% nickel (Ni) into Pb-free solders has been identified as a transformative approach. Research findings highlight substantial changes in the microstructure of Cu-Sn intermetallic compounds (IMCs) resulting from Ni's solubility in (Cu,Ni)-Sn IMCs, replacing Cu atoms, has a noticeable impact on the mechanical, thermal, and wettability properties of joints on Cu substrates (Hammad, 2013; Laurila, Vuorinen, & Paulasto-Kröckel, 2010; Somlyai-Sipos, & Baumli, 2017; Xian et al., 2018; Yang, Song, & Lee, 2014; Yao, Liu, & Liu, 2009; Zeng et al., 2014). In response to these challenges, the effect of Ni microalloying in the In-35Sn solder during the reflow process on Cu substrate need to be explored.

Moreover, as the electronic packaging industry trends towards device miniaturization and system integration, including stacked Package-on-Package (POP) or System-in-Package (SiP), the assembly of circuit boards requires multiple reflow processes. Yet, these processes impact microstructure evolution and introduce new reliability challenges (Haseeb, Leong, & Arafat, 2014; Huang et al., 2019; Liu, Chen, Liu, Wu, & An, 2016). It is essential to investigate the effects of Ni microalloying on the microstructural characteristics, mechanical properties, and soldering performance of In-

35Sn solder alloys during multiple reflow cycles for ensuring solder joint reliability and reducing manufacturing costs.

1.3 Research objectives

This research is dedicated to investigating the potential of the In-35 wt%Sn solder alloy, particularly with the addition of 0.05 wt% nickel (Ni) microalloying. This alloy system holds promise as a potential low-temperature lead-free solder, offering advantages in terms of cost-effectiveness in manufacturing process, reduced thermal risks to temperature-sensitive components and utilized in the flexible electronics industry. The research objective is to delve into the effect of Ni microalloying on the microstructure formation during solidification, a fundamental process that underpins various soldering operations and their effect to the mechanical properties. This research aims to investigate the following main objectives:

i) To investigate the detailed examination of the solidification process of In-35 wt%Sn solder alloys through real-time synchrotron X-ray imaging. Specifically, the effect of Ni microalloying on the microstructure formation and solidification behaviour in the In-35 wt%Sn solder will be observed.

ii) To investigate the influence of Ni microalloying on the interfacial reactions that occur between In-35 wt%Sn solder bumps and copper (Cu) substrates during reflow soldering.

iii) To investigate the nucleation and kinetic growth behaviour of intrinsic Ni microalloying within the In-35 wt%Sn bulk solder alloy and interfacial IMC during multiple reflow soldering cycles on Cu substrates. This effect of microstructure formation on the mechanical reliability of solder joints will also be explored.

1.4 Research scope

This study focuses on the effect of 0.05 wt% nickel (Ni) microalloying in the In-35Sn (wt%) bulk solder alloy and when soldered on copper (Cu) substrates. The research comprises three distinct phases:

First phase: Investigation on the properties of the In-35Sn and In-35Sn-0.05Ni solder systems. This phase encompassed casting the solder alloys, conducting in-situ real-time observations of microstructure evolution during solidification using synchrotron X-ray radiography imaging, correlating solidification temperatures by differential scanning calorimeter (DSC) analysis, determining the alloys' solidification paths and chemical compounds formed using the TCSLD v3.3 database in ThermoCalc®, and performing ex-situ microstructure examinations using scanning electron microscope (SEM) with energy dispersive X-ray analysis.

Second phase: Examination of the microstructure and mechanical properties of In-35Sn and In-35Sn-0.05Ni solder joints on Cu substrates through reflow soldering. The in-situ microstructure formation during reflow soldering will be observed using synchrotron X-ray radiography imaging. The interfacial IMC layer will be characterized

using focused ion beam scanning electron microscope (FIB-SEM) with EDX, and further grain structure analysis will be conducted through transmission electron microscope (TEM). Mechanical properties will be assessed by high-speed shear (HSS) solder ball test using a Dage 4000 high-speed bond tester.

Third phase: Investigation of microstructure and mechanical properties of In-35Sn and In-35Sn-0.05Ni solder joints on Cu substrates over six reflow cycles. The in-situ synchrotron X-ray radiography imaging technique will be employed to visualize microstructure evolution during multiple reflow cycles. Ex-situ microstructure analysis of bulk solder and solder joint interfaces will be carried out using field emission scanning electron microscope (FESEM). The solidification temperature analysis during six reflow cycles will be performed via DSC, and the mechanical strength will be determined through HSS solder ball test.

1.5 Thesis outline

The thesis adopts a structure that aligns with the research objectives:

Chapter 1: Introduction – This chapter introduces the research background, outlines the objectives of the study, and provides an overview of the thesis' organization.

Chapter 2: Literature review – A comprehensive review of the development of lead-free solder alloys and their behaviour in solder joints on copper substrate.

Chapter 3: Published Papers – This chapter provides an overview of the paper published in the journal indexed on the Web of Science (WoS). It presents three published papers coherently, aligning with the objective of this research study.

Chapter 4: Summary and future work – Summarizes findings, draws conclusions, and provides recommendations for future research directions.

CHAPTER 2 : LITERATURE REVIEW

Soldering has a long history and has attracted considerable interest, particularly in the development of electronics assembly field. This chapter presents an extensive review of current studies in the development of solder interconnects in advanced electronic packaging. It covers the topics such as low temperature lead-free solder, multiple reflow processes, the effects of Ni microalloying on lead-free solder, solidification reactions, interfacial reactions of the solder and a copper substrate, and the implications for solder joint reliability.

2.1 Solder in electronic packaging

Solder is a fusible metal or alloy that widely used for assembly of electronic devices through the soldering process, which creates metallurgical bonds for joining components to printed circuit boards (PCBs), enabling the expansion and contraction of various components, dissipating heat, and transmitting electrical signals. This process involved four basic elements which are base metal, flux, solder, and heat. Through heat application, solder alloys are melted at relatively low temperatures to form metallurgical bonds between two metals. The properties of solder are important to ensure the reliability of the solder joint, ultimately influencing the overall functionality of electronic devices.

As microelectronics packaging evolves to accommodate higher packaging density, improved performance, miniaturization, and efficient space utilization in electronic products, solder bump techniques have become pivotal in solder joint formation in electronic assemblies. The concept of Moore's Law underscores the

exponential growth in computing power and component miniaturization. However, a foreseen plateau in the miniaturization aspect of Moore's Law looms, attributed to the physical constraints that impede further reduction in component size on a chip (Tozzi, May, 26 2023). To surmount this challenge, three-dimensional integrated circuit (3D-IC) technology emerges as a promising solution. Techniques such as interposer, through-silicon-via (TSV), and micro-bump (μ-bump) methods contribute to stacked chip integration, enabling higher density and functionality (Liu, Chu, & Tu, 2016; Liu et al., 2020; Zhang et al., 2022).

The 3D-IC techniques enable the vertical stacking of chips to further enhance computing power and functionality in miniaturization package, as shown in Figure 2.1. In this techniques, vertical interconnections between chips and substrates are achieved using solder bumps of varying sizes, ranging from approximately 760 μm to 20 μm. These solder bumps consist of three different sizes: the largest being the ball-grid-array (BGA), followed by the intermediate-sized controlled-collapse-chip-connection (C-4) flip chip solder bumps, and finally the smallest being the μ-bump (Liu, Chu, et al., 2016). The adoption of flip chip package technology in the current electronic packaging industry has significantly reduced the size of solder joints compared to ball grid array (BGA) structures (Chen et al., 2017), enabling higher density and more functional advanced electronic packaging (Kang et al., 2007). This integration trend has led to increased device density, faster speeds, and reduced power consumption in denser packages.

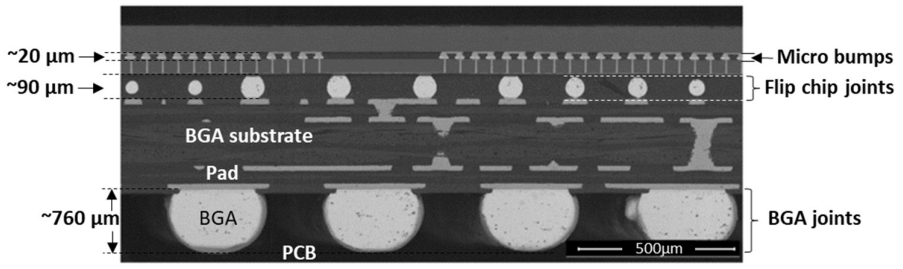

Figure 2.1 Cross-sectional view of vertical stacking of chips in 3D IC sample (Liu et al., 2020)

Similarly, as shown in Figure 2.2, the advancement of Fan-Out Wafer-Level Package (FO-WLP) techniques offers the potential to improve production efficiency by integrating multiple smaller dies instead of larger ones. An example of a 3D FO-WLP configuration is the Package-on-Package (PoP) method, which enables the creation of thin-shell, high-performance storage (Zhang et al., 2022).

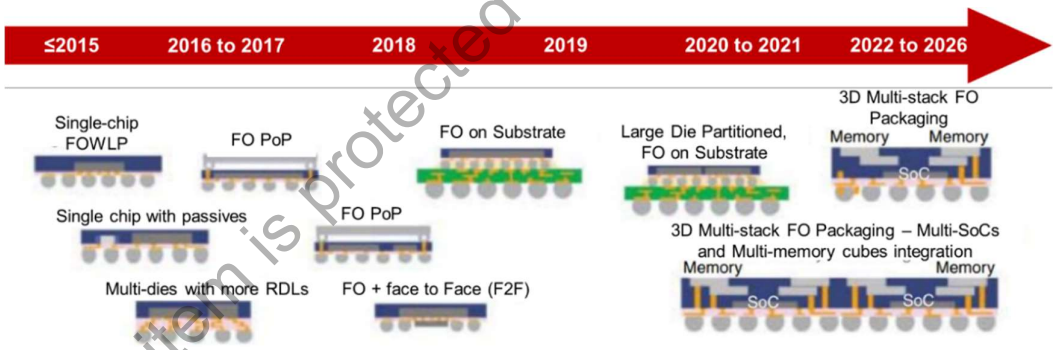

Figure 2.2 The development of FO-WLP integration (Zhang et al., 2022)

Throughout the history of electronic assembly history, tin-lead (Sn-Pb) is the ubiquitous solder alloy provides compatibility with a wide range of electronic components and substrate materials. It has advantages such as a low melting point (eutectic Sn-37Pb, 183 °C), facilitating manufacturing processes, as well as good ductility, wettability, reliability, and affordability (Cheng et al., 2017). However, concerns over the toxicity of Pb to human health and its environmental impact prompted directives like the European Union Waste Electrical and Electronic Equipment Directive