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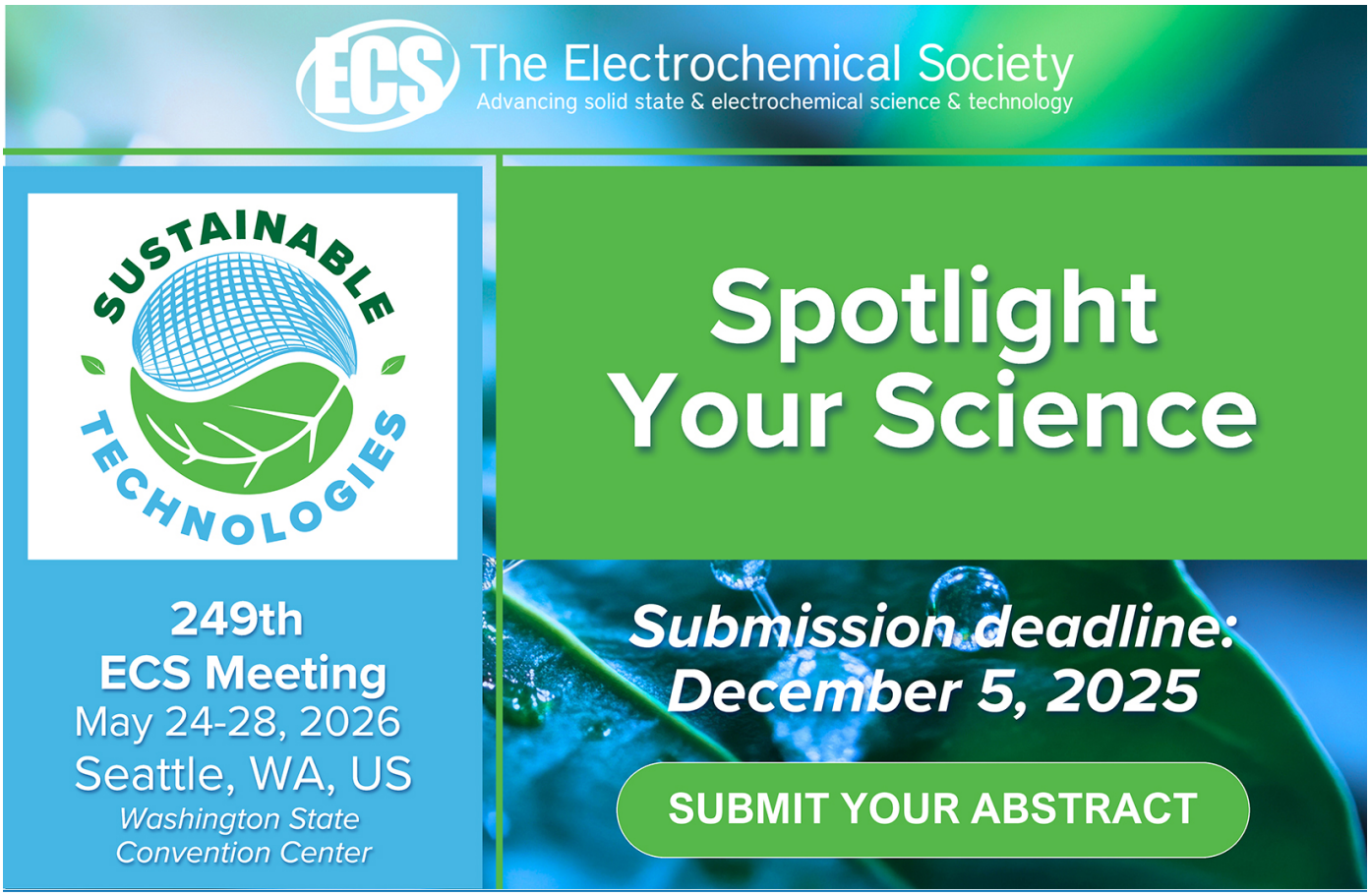

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# Design and Development of Two-stage Low-noise Amplifier (LNA) using E-pHEMT Technology for C-band Application

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**Abstract.** The low-noise amplifier (LNA) is a vital part of the radio frequency (RF) transceiver system. It amplifies weak signals with minimal distortion. The LNA performance is mainly determined by its noise figure (NF), gain, and power consumption. In this paper, the design of a 6 GHz low-noise amplifier (LNA) using enhancement-mode pseudomorphic high-electron-mobility transistor (E-pHEMT) technology is presented. In order to attain high gain with low *S*-parameters losses, a two-stage LNA configuration with single-stub matching is devised. The same bias conditions are applied to both of the LNA stages, $V_{DS}$ = 2.7 V and $I_{DS}$ = 10 mA. The LNA design is simulated and optimised by using electromagnetic (EM) software. To further improve the overall LNA performances, high impedance inductors and series resonators are implemented into the circuit. Simulated results of the designed LNA indicate a power gain, $S_{21}$ of 25.2 dB and NF of 2.4 dB at 6 GHz with 27 mW dissipation per stage. The circuit layout is fulfilled with an E-pHEMT technology (ATF-55143) on the FR4 substrate. The LNA is powered by a 3 V DC power supply.

## 1. Introduction

Wireless communication is a widely implemented form of communication systems. It is extremely well-liked as it offers mobility at a low cost [1]. The low-noise amplifier (LNA) is a critical primary section of the radio frequency (RF) transceiver system. It amplifies a very low-power signal with minimal additive distortion [2]. The standard LNA configuration includes the input and output matching network, and transistor amplifier [3].

The LNA is a small-signal amplifier with moderate gain and the least possible noise figure (NF) [4]. However, it is quite challenging to synchronously realise low noise and maximum gain. Trade-offs are required to be made to acquire low noise and high gain. The main requirements to verify the LNA performance quality are gain, voltage standing wave ratio (VSWR) and NF [5]. An LNA is also expected to have a good impedance matching, stability, and linearity within its operation band [6]. Applications of LNAs include wireless local area networks (WLANs), Bluetooth, global positioning system (GPS), and satellite communications.

E-pHEMT-based LNAs have gained great interest due to their low-noise intrinsic traits [7-8]. The E-pHEMT devices provide low noise, high gain, high reliability, high linearity, and high transconductance

[9-10]. The C-band LNAs are extensively applied since they offer low-noise performance, high data rate, and high speed with reduced power dissipation [11].

In 2019, Kumar and Deolia designed a low-power, wideband LNA using particle swarm optimisation with a power gain, $S_{21}$ of 16.6 dB and NF of 2.4 dB at 25.4 GHz [12]. A GaN monolithic microwave integrated circuit (MMIC) LNA design proposed by Kazan, Kocer, and Civi has obtained $S_{21}$ of 22.0-30.8 dB and NF of 1.60-1.95 dB over the frequency range of 8-11 GHz [13]. A GaAs field-effect transistor (FET) LNA designed by Iyer and Shanmuganantham revealed to attain an $S_{21}$ of 10.3 dB and NF of 5.2 dB at 3.5 GHz [15]. Xia, Dai, Li, Lyu, and Xu introduced an LNA using D-pHEMT technology in 2018 with $S_{21}$ of 18 dB and NF of 1.9 dB from 6-18 GHz [16].

This paper focuses on the design of a two-stage LNA using E-pHEMT technology. Single-stub matching networks on both sides of the transistor amplifier are designed and developed into the LNA circuitry to attain accurately matched impedances for improved *S*-parameter performance. DC bias is incorporated into the LNA system. High-impedance inductors are positioned at the drain and gate of the transistor amplifier to prevent microwave signals from entering the DC power supply. The proposed LNA is designed for operation at 6 GHz which resides in the C-band frequency range. This specific band is applicable for wireless and satellite communications, and radiolocation implementations [17]. The LNA is designed and optimised in an electromagnetic (EM) software. Simulated results of the proposed two-stage C-band LNA are presented.

## 2. Methodology

### *2.1. Transistor Amplifier Stability Test*

The first step in LNA design procedure is to select a suitable transistor amplifier. The transistor amplifier requires to be carefully reviewed while considering the LNA design trade-offs since the LNA should deliver a high gain and low noise figure NF at a low current intake i.e. low power consumption [14,18].

The stability of the transistor amplifier is verified based on its *S*-parameters using Rollet's stability factor given by (1) and (2). It is important to determine the stability at the initial stage to comprehend the condition of the transistor amplifier. It is unconditionally stable if $K$ is larger than unity ($K > 1$) while it is only conditionally stable if the $K$ is smaller than unity ($K < 1$). Plotting stability circles on the Smith chart is essential to verify areas in which the LNA is unstable to prevent oscillation.

Rollet's stability factor expressed in [17] is specified as

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{1}$$

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} \geq 1 \tag{2}$$

The selected transistor amplifier (ATF-55143) has a stability factor, $K$ of 1.04 at 6 GHz. Hence, it is unconditionally stable for any source and load impedance arrangements. Figure 1 shows the simulated stability factor, $K$ of ATF-55143.

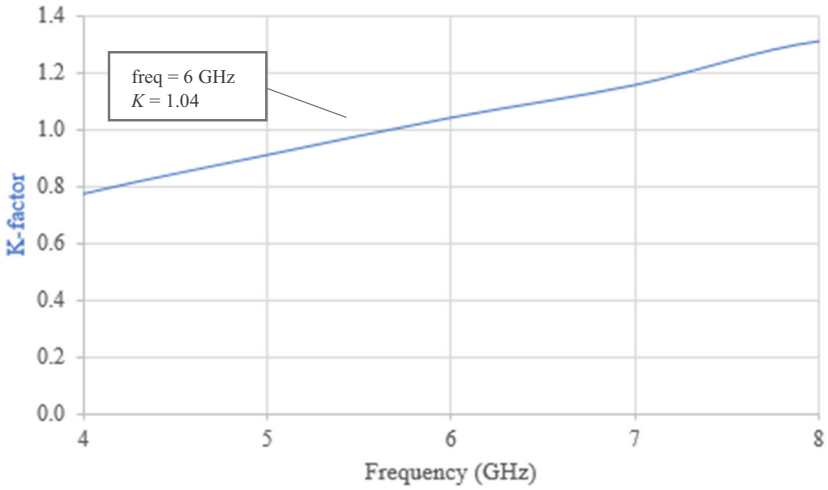


**Figure 1.** Simulated stability factor, *K* of ATF-55143

*2.2. Transistor Amplifier Biasing*

By referring to the stability test result, biasing conditions for the LNA are set. Bias points of the ATF-55143 are selected by following the datasheet to operate at $V_{DS}$ = 2.7 V and $I_{DS}$ = 10 mA. The DC bias is calculated using passive biasing calculations. The values of the circuit are $V_{DD}$ = 3 V, $V_{DS}$ = 2.7 V, $I_{DS}$ = 10 mA, $V_{GS}$ = 0.47 V, and $I_{BB}$ = 0.5 mA.

$$R_3 = \frac{V_{DD} - V_{DS}}{I_{DS} + I_{BB}} \tag{3}$$

$$R_1 = \frac{V_{GS}}{I_{BB}} \tag{4}$$

$$R_2 = \frac{(V_{DS} - V_{GS})R_1}{V_{GS}} \tag{5}$$

The bias circuit incorporates resistors between the drain and gate of the ATF-55143, and DC power supply, which embody a voltage divider network. The resistors are coupled with a series capacitor, $C_1$ = 1 µF. The DC bias circuit structure is built and simulated by using an EM simulator. Resistor values are calculated as $R_1$ = 4750 Ω, $R_2$ = 30 Ω, $R_3$ = 1 kΩ, and $R_4$ = 10 kΩ to obtain the required bias points. Figure 2 shows the bias circuit with a 3 V DC power supply.

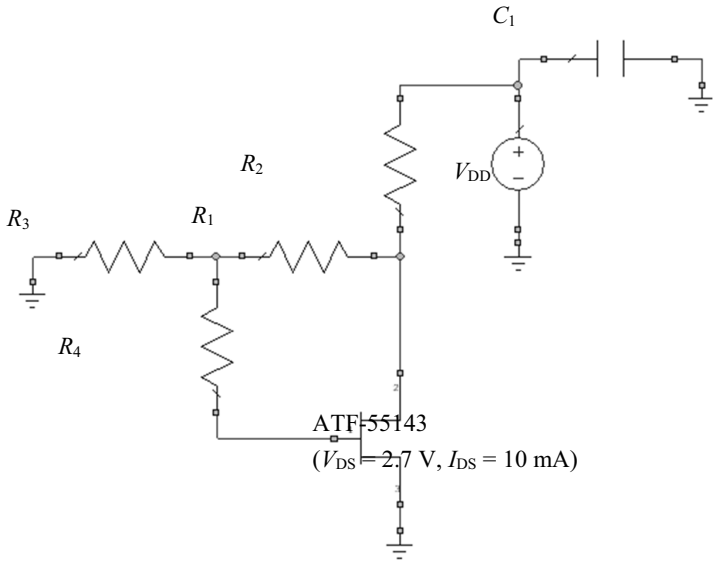


**Figure 2.** DC bias circuit with bias points $V_{DS}$ = 2.7 V and $I_{DS}$ = 10 mA

*2.3. Low-noise Amplifier Design*

Unilateral amplifier design is adopted while designing impedance matching circuits of the LNA. According to the unilateral amplifier design rule, when $S_{12} = 0$,

$$\Gamma_{\text{in}} = S_{11} \tag{6}$$

$$\Gamma_{\text{out}} = S_{22} \tag{7}$$

Consequently, the unilateral transducer gain, $G_{\text{TU}}$ is defined as $G_{\text{T}}$ when $S_{12} = 0$ [18].

$$G_{\text{TU}} = |S_{21}|^2 \frac{1-|\Gamma_{\text{S}}|^2}{|1-S_{11}\Gamma_{\text{S}}|^2} \frac{1-|\Gamma_{\text{L}}|^2}{|1-S_{22}\Gamma_{\text{L}}|^2} \tag{8}$$

Meanwhile, the noise figure (NF) of a two-port active device is written as

$$F = F_{\text{min}} + 4\frac{\text{R}_{\text{n}}}{\text{Z}_0} \frac{|\Gamma_{\text{S}}-\Gamma_{\text{opt}}|^2}{|1+\Gamma_{\text{opt}}|^2(1-|\Gamma_{\text{S}}|^2)} \tag{9}$$

The LNA is implemented as a two-stage amplifier. The two stages are connected by a coupling capacitor, $C_3$ = 1 μF. The capacitor delivers the amplified signal from the first transistor amplifier to the second transistor amplifier.

50 Ω load terminations are operated to calculate *S*-parameters of the network. Smith chart matching impedances are drawn and calculated to acquire the length and width of the transmission lines and stubs for both input and output matching impedances.

From the Smith chart design, length and width of the transmission lines and stubs at the input and output sections are slightly optimised to obtain the best *S*-parameters performance. The values for input matching are $l_1$ = 21 mm, $w_1$ = 2 mm, $l_2$ = 16 mm, $w_2$ = 3.7 mm, $l_3$ = 8.1 mm, $w_3$ = 2.6 mm, $l_4$ = 7.9 mm, and $w_4$ = 4.6 mm after optimisation. The optimised values for output matching are $l_5$ = 17 mm, $w_5$ = 3 mm, $l_6$ = 27 mm, $w_6$ = 3 mm, $l_7$ = 15.5 mm, $w_7$ = 3 mm, $l_8$ = 11.5 mm, and $w_8$ = 3 mm respectively. All widths at the output section are the same since they are designed at 50 Ω terminations.

The LNA circuit is designed on FR4 with specifications of relative permittivity, $\varepsilon_r$ = 4.6, substrate thickness, $H$ = 1.6 mm, copper thickness, $T$ = 0.035 mm, and dielectric loss, tan $\delta$ = 0.01 according to [20]. A complete schematic diagram of the proposed two-stage LNA is shown in figure 3.

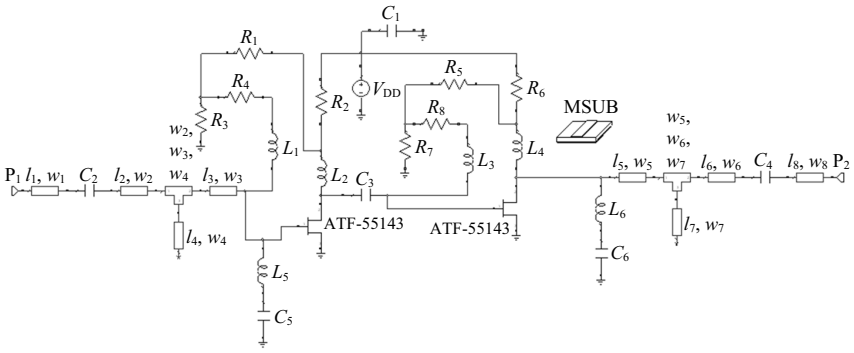


**Figure 3.** Schematic diagram of the proposed two-stage LNA

## 3. Results and Discussion

At 6 GHz, impedances of the inductors i.e. $L_1$, $L_2$, $L_3$, and $L_4$ are increased and the DC bias network i.e. $R_1$, $R_2$, $R_3$, $R_4$, $R_5$, $R_6$, $R_7$, and $R_8$ are entirely separated from the matching impedance network (transmission lines and stubs). Thus, a purely matched input and output for the source and load of the LNA is achieved. When high-frequency signals are fed into the input terminal of the ATF-55143, the inductors act as chokes where they prevent the AC signal from passing through the DC power supply, $V_{DD}$.

Series resonators i.e. $L_5$, $C_5$ and $L_6$, $C_6$ are located at the input and output terminal of the LNA. The series peaking inductors $L_5$ and $L_6$ are utilised to suppress the influence of gate-source capacitance of $C_5$ and drain-source capacitance of $C_6$ as well as Miller effect of the hybrid gate to drain capacitances [13]. This remarkably assists to broaden the wideband input and output matching as well as improve the overall power gain and NF performance of the LNA.

The simulated frequency bandwidth is from 5.8 GHz to 6.2 GHz i.e. 400 MHz. Figure 4 shows the simulated results of the input reflection coefficient, $S_{11}$ and output reflection coefficient, $S_{22}$. The simulated $S_{11}$ is below -8.0 dB across the bandwidth. Meanwhile, at 6 GHz (centre frequency), the $S_{11}$ is -11.5 dB. The $S_{22}$ is well below -10 dB across the bandwidth. The value of $S_{22}$ at 6 GHz is -14.2 dB.

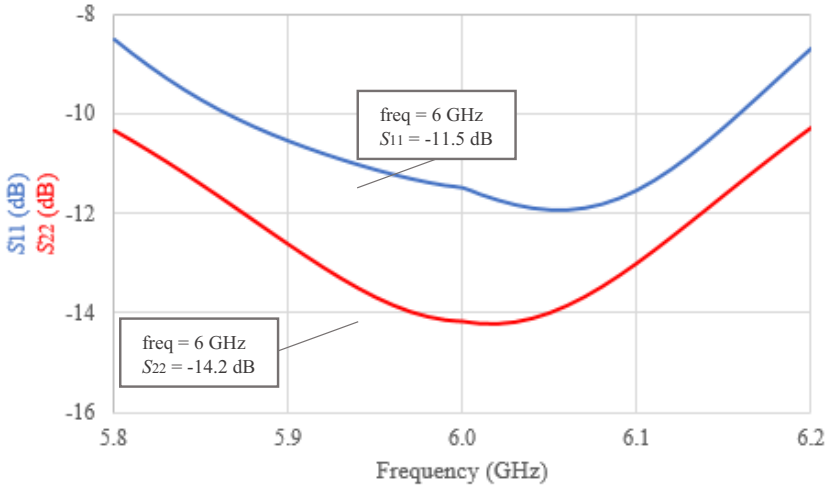


**Figure 4.** Simulated input and output reflection coefficients, $S_{11}$ and $S_{22}$

As shown in figure 5, the simulated power gain, $S_{21}$ is maintained above 23.5 dB across the whole frequency bandwidth. At 6 GHz, the $S_{21}$ is 25.2 dB.

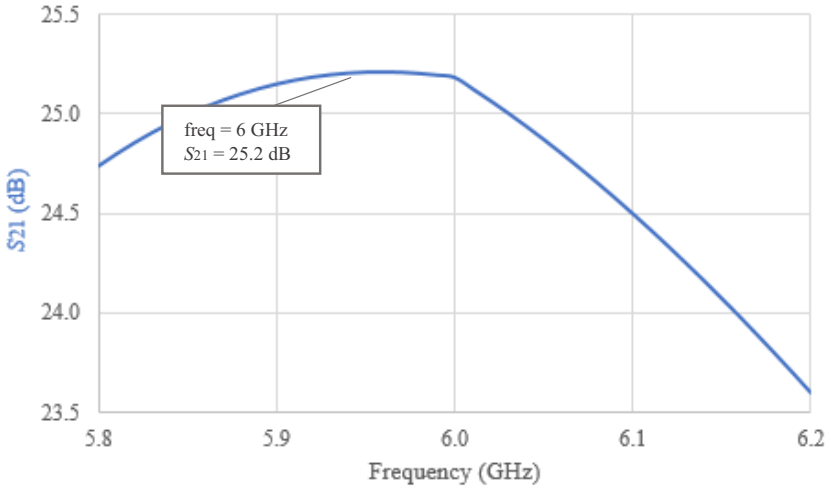


**Figure 5.** Simulated power gain, $S_{21}$

Figure 6 shows the simulated noise figure (NF). The NF is below 3 dB across the bandwidth. The LNA has an NF of 2.4 dB at 6 GHz.

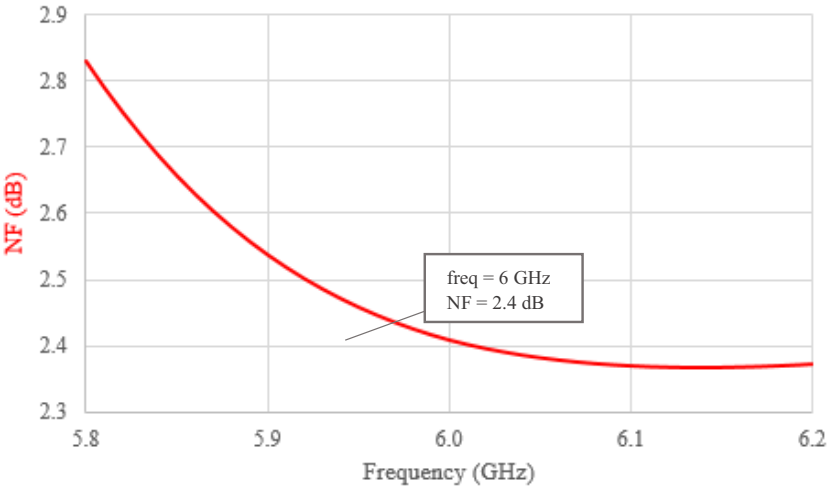


**Figure 6.** Simulated noise figure (NF)

Table 1 outlines the performance comparison of the designed LNA with other similar, published studies. The reviewed characteristics of the LNAs include frequency operation, input reflection coefficient, $S_{11}$, output reflection coefficient, $S_{22}$, power gain, $S_{21}$, noise figure (NF), power consumption, and technology.

**Table 1**. LNA performance comparison summary

| Parameters | Proposed work | [12] | [13] | [14] | [15] |
|---|---|---|---|---|---|
| Frequency | 5.8-6.2 GHz | 0-35 GHz | 8-11 GHz | 3.4-3.6 GHz | 6-18 GHz |
| Input reflection coefficient, $S_{11}$ | -11.5 dB | < -10.9 dB | 9.1-20.6 dB | -5.8 dB | -10.0 dB |
| Output reflection coefficient, $S_{22}$ | -14.2 dB | N.A. | N.A. | N.A. | < -10.0 dB |
| Power gain, $S_{21}$ | 25.2 dB | > 13.6 dB | 22.0-30.8 dB | 10.3 dB | 18.0 dB |
| Noise figure (NF) | 2.4 dB | 2.4-3.1 dB | 1.6-2.0 dB | 5.2 dB | 1.9 dB |
| Power consumption | 54.0 mW | 1.6 mW | 600.0 mW | N.A. | 367.5 mW |
| Technology | GaAs pHEMT | 45.0 nm CMOS | GaN/SiC HEMT | GaAs FET | GaAs pHEMT |

## 4. Conclusion

A two-stage LNA for C-band application operating at 6 GHz has been presented in this paper. The designed LNA has a wideband frequency range from 5.8 GHz to 6.2 GHz. The ATF-55143 is operated at $V_{DS}$ = 2.7 V and $I_{DS}$ = 10 mA to comply with its DC bias characteristics. Smith charts are employed to achieve a matched input and output impedance networks. The input and output matching networks are designed by applying single open-circuited stub. Inductors are included in the DC bias circuit to isolate it from the matching impedance layout circuit to incite a better power gain. Series resonator circuits are used to improve matching impedance, NF, and power gain of the LNA. EM software is utilised to design and simulate the proposed LNA. The simulated input and output reflection coefficients, $S_{11}$ and $S_{22}$ at 6 GHz are -11.5 dB and -14.2 dB respectively. A power gain, $S_{21}$ of 25.2 dB is obtained from the LNA simulation, with an NF of 2.4 dB. The LNA consumes 27 mW per stage from a 3 V DC supply.

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