



**NUMERICAL SIMULATIONS OF INNOVATIVE
GROUND PLANE AND DOUBLE-GATE
CONFIGURATIONS IN THIN-BODY AND –
BURIED OXIDE OF SOI MOSFETs**

by

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TABLE OF CONTENTS

	PAGE
DECLARATION OF THESIS	i
ACKNOWLEDGEMENT	ii
TABLE OF CONTENTS	iv
LIST OF TABLES	vii
LIST OF FIGURES	viii
LIST OF ABBREVIATIONS	xiv
LIST OF SYMBOLS	xvi
ABSTRAK	xix
ABSTRACT	xx
CHAPTER 1 INTRODUCTION	1
1.1 General review of CMOS Technology	1
1.1.1 Scaling of CMOS Technology to Their Limits	1
1.1.2 Scaling Challenges	3
1.1.3 Advanced CMOS Technology	4
1.2 Research Scope	10
1.3 Research Objectives	11
1.4 Organization of the Thesis	12
CHAPTER 2 LITERATURE REVIEW	14
2.1 Silicon-on-Insulator (SOI)	14
2.1.1 SOI versus Bulk	14
2.1.2 Thin -body and -buried oxide of SOI transistor	19

2.1.3	Implementation of ground plane (GP)	22
2.2	Multiple-gate transistors	24
2.2.2	Advantages of multiple-gate transistors	24
2.2.3	Single-gate (SG) vs double-gate (DG)	25
CHAPTER 3 METHODOLOGY		28
3.1	Simulation Methodology	28
3.2	Selection of Numerical Methods and Physical Models	29
3.3	Simulated Device Structures	31
3.4	Measurements and Parameter Extractions	34
3.4.1	DC Parameter Extractions	34
3.4.2	Analog/RF Parameter Extractions	34
CHAPTER 4 RESULTS & DISCUSSIONS		45
4.1	Ultra-thin body (UTB) vs ultra-thin body and BOX (UTBB)	45
4.1.1	$V_{\text{Sub}} = 0.5 \text{ V}$	48
4.1.2	$V_{\text{Sub}} = -2.0 \text{ V}$	51
4.1.3	$V_{\text{Sub}} = 2.0 \text{ V}$	53
4.1.4	Summary	57
4.2	Ultra-thin body and BOX (UTBB) at $L_g = 25 \text{ nm}$	57
4.2.1	Results of digital FoM	58
4.2.2	Results of analog/RF FoM	62
4.2.3	Summary	75
4.3	Ultra-thin body and BOX (UTBB) at $L_g = 10 \text{ nm}$	76
4.3.1	Variations in GP architectures and gate configurations (SG vs DG)	76
4.3.2	Variations in GP architectures and silicon-body thickness (T_{si})	87
4.3.3	Variations in GP architectures and dielectric materials	94
4.4	Benchmarking of transistor's figure-of-merits (FoM)	100

CHAPTER 5 CONCLUSIONS	104
5.1 Contributions of this research work	104
5.2 Directions for future work	107
REFERENCES	110
APPENDIX	127

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LIST OF TABLES

NO.		PAGE
Table 1.1:	The classical scaling trends	2
Table 3.1:	Device parameters used to evaluate the performance of UTBB SOI MOSFETs in this work	34
Table 4.1:	<i>DIBL</i> for UTBB SOI MOSFETs ($L_g = 25$ nm) for different GP architectures	60
Table 4.2:	<i>DIBL</i> for UTBB SOI MOSFETs ($L_g = 10$ nm) for different GP architectures	80
Table 4.3:	Results of subthreshold swing (<i>SS</i>) (mV/dec) at $V_d = 20$ mV	90
Table 4.4:	Results of I_{on} (A/ μ m)	91
Table 4.5:	Results of I_{off} (A/ μ m).	91
Table 4.6:	Dielectric materials and its thickness used in the simulations	95
Table 4.7:	Results of <i>SS</i> (mV/dec) for DG UTBB SOI MOSFETs	98
Table 4.8:	Summary of device electrostatic features and analog FoM for our simulated work ($L_g = 25$ nm, SG) against experimental results	101

LIST OF FIGURES

NO.		PAGE
Figure 1.1:	Principles of MOSFET constant-field scaling (Davari, Dennard, & Shahidi, 1995)	2
Figure 1.2:	Limits of downscaling (Ahmad & Schuegraf, 2011)	4
Figure 1.3:	(a) Evolution of transistor in each technology nodes for continuous improvements of performances (M. Bohr & Mistry, 2011) (b) Optimizing choices on multiple areas to sustain downscaling beyond 5 nm (Mistry, 2014)	8
Figure 1.4:	Evaluation of potential solutions for extending CMOS scalability (“International Technology Roadmap for Semiconductors (ITRS),” 2009)	9
Figure 1.5:	Major challenges and possible technical solutions for extending CMOS scalability (Hiramoto, 2009, 2011)	9
Figure 2.1:	Configuration of (a) bulk and (b) SOI MOSFET devices	14
Figure 2.2:	Illustration of electric field distribution from the source and drain toward the channel region for (a) bulk silicon and (b) FD-SOI MOSFETs (Md Arshad, 2013)	16
Figure 2.3:	Ultra-thin body (UTB) versus ultra-thin body and BOX (UTBB) structures (Noraini Othman, Md Arshad, & Sabki, 2017)	21
Figure 2.4:	Comparison of the <i>DIBL</i> for NMOS and PMOS devices for wafers with thin BOX with and without GP and thick BOX (Fenouillet-Beranger et al., 2009)	22
Figure 2.5:	Field penetration in the body controlling the body potential of (a) standard SOI MOSFET and (b) SOI MOSFET with a GP (T Ernst et al., 2002)	24

Figure 2.6:	Structures of various SOI transistors: (a) single-gate (b) double-gate (c) double-gate non-planar FinFET (d) tri-gate FET (e) quadruple-gate (or gate-all-around) FET and (f) gate-all-around (or surrounding gate) FET (nanowire FET) (Kim, 2010)	25
Figure 3.1:	Schematics of (a) UTB vs. (b) UTBB devices	33
Figure 3.2:	Schematic cross-sectional structures of UTBB SOI MOSFETs of $L_g = 25$ nm with different GP architectures (a) no-GP (b) std-GP (c) GP-A and (d) GP-B	33
Figure 3.3:	UTBB SOI MOSFETs showing DG device configurations with synchronize gate voltage where $V_{\text{top-gate}} = V_{\text{top-GP}}$	34
Figure 3.4:	MOSFET transfer characteristics showing I_d (on a logarithmic scale on the left and a linear scale on the right) versus V_g used to extract various electrostatic parameters	35
Figure 3.5:	Various V_{th} extraction methods (a) constant current (CC) method (b) extrapolation of linear region (ELR) method (c) transconductance linear extrapolation (GMLE) method (d) second derivative (SD) method (e) ratio method (RM) and (f) second derivative logarithmic (SDL) method (Ortiz-Conde et al., 2002)	37
Figure 3.6:	Conduction band profile along the position in channel for 20 mV and 1 V drain voltages (linear and saturated case)	39
Figure 3.7:	Transfer curve showing $DIBL$ extracted as $DIBL = (\Delta V_{\text{th}}/\Delta V_d) = (V_{\text{th}1} - V_{\text{th}2} / (V_{\text{d}2} - V_{\text{d}1}) = (V_{\text{th}(\text{linear})} - V_{\text{th}(\text{saturation})} / (V_{\text{drain}(\text{saturation})} - V_{\text{drain}(\text{linear})})$	39
Figure 4.1:	Normalized I_d - V_g curve for a SG UTBB SOI MOSFETs obtained in (a) experimental work reported in Md Arshad (2013) of $L_g = 30$ nm and (b) our simulation work of $L_g = 25$ nm	46
Figure 4.2:	$DIBL$ as a function of V_{Sub} extracted at $I_d = 10^{-7}$ A for ultra-thin body (UTB) and ultra-thin body and BOX (UTBB) SOI MOSFETs	48

- Figure 4.3: Surface potential ($\psi_s = \psi_{\text{Horizontal}} - (V_{\text{Sub}} - \Phi_F)$) cut at the interface of BOX/substrate at $V_{\text{Sub}} = 0.5$ V for UTB and UTBB SOI MOSFETs 50
- Figure 4.4: Vertical potential (ψ_{Vertical}) cut through the top-gate and into the channel, BOX and substrate near the source at $V_{\text{Sub}} = 0.5$ V for UTB and UTBB SOI MOSFETs 51
- Figure 4.5: Surface potential ($\psi_s = \psi_{\text{Horizontal}} - (V_{\text{Sub}} - \Phi_F)$) cut at the interface of BOX/substrate at $V_{\text{Sub}} = -2.0$ V for UTB and UTBB SOI MOSFETs 52
- Figure 4.6: Vertical potential (ψ_{vertical}) cut through the top-gate and into the channel, BOX and substrate near the source at $V_{\text{Sub}} = -2.0$ V for UTB and UTBB SOI MOSFETs 53
- Figure 4.7: Surface potential ($\psi_s = \psi_{\text{Horizontal}} - (V_{\text{Sub}} - \Phi_F)$) cut at the interface of BOX/substrate at $V_{\text{Sub}} = 2.0$ V for UTB and UTBB SOI MOSFETs 54
- Figure 4.8: Vertical potential (ψ_{vertical}) cut through the top-gate and all the way into the channel, BOX and substrate near the source at $V_{\text{Sub}} = 2.0$ V for UTB and UTBB SOI MOSFETs 56
- Figure 4.9: Surface potential ($\psi_s = \psi_{\text{Horizontal}} - (V_{\text{Sub}} - \Phi_F)$) cut at interface of BOX / substrate and at $V_{\text{Sub}} = 0.0, 0.5, 2.0$ and -2.0 V for ultra-thin-BOX (UTBB) SOI MOSFETs 56
- Figure 4.10: I_d - V_g transfer characteristics for a std-GP SG UTBB SOI MOSFETs obtained in our simulation work of $L_g = 25$ nm at $V_d = 50$ mV and $V_d = 1$ V 59
- Figure 4.11: Plot of I_d - V_g for UTBB SOI MOSFETs of $L_g = 25$ nm with *DIBL* extracted as $= (V_{\text{th(Linear)}} - V_{\text{th(saturation)}}) / (V_{\text{drain(saturation)}} - V_{\text{drain(linear)}})$ 61

- Figure 4.12: Transconductance (g_m) for a SG UTBB SOI MOSFET of std-GP with $L_g = 25$ nm and $W = 1$ μ m obtained from (a) DC simulations where $g_m = dI_d/dV_g$ and (b) AC simulations where $g_m = |Y_{21} - Y_{12}|$ 63
- Figure 4.13: $g_{m_max}/(W/L)$ as a function of frequency for (a) single-gate (SG) and (b) double-gate (DG) modes. $L_g = 25$ nm, $W = 1$ μ m and $V_d = 1$ V 66
- Figure 4.14: Simulated g_d as a function of frequency for (a) (i) SG and (ii) its corresponding zoom-in view and (b) (i) DG and (ii) its corresponding zoom-in view. $L_g = 25$ nm, $W = 1$ μ m and $V_d = 1$ V 69
- Figure 4.15: Simulated A_v as a function of frequency where $A_v = 20 \cdot \log(g_m/g_d)$ for (a) SG and (b) DG modes. $L_g = 25$ nm, $W = 1$ μ m and $V_d = 1$ V 70
- Figure 4.16: Simulated C_{gg} as a function of frequency for (a) SG and (b) DG modes. $L_g = 25$ nm, $W = 1$ μ m and $V_d = 1$ V 72
- Figure 4.17: Simulated f_t as a function of frequency for (a) SG and (b) DG modes. $L_g = 25$ nm, $W = 1$ μ m and $V_d = 1.0$ V 74
- Figure 4.18: Plot of I_d-V_g for UTBB SOI MOSFETs of $L_g = 10$ nm for various GP architectures with respect to SG and DG operation modes for (a) std-GP (b) GP-A and (c) GP-B 79
- Figure 4.19: Horizontal potential ($\psi_{Horizontal}$) cut at the interface of BOX/substrate of $L_g = 10$ nm for SG and DG of UTBB SOI MOSFETs 80
- Figure 4.20: Vertical potential ($\psi_{Vertical}$) cut near the source and into the gate, channel, BOX and substrate of $L_g = 10$ nm (a) SG and (b) DG for UTBB SOI MOSFETs 81
- Figure 4.21: Subthreshold swing (SS) for SG and DG operation-mode at (a) $V_d = 20$ mV and (b) 1 V 83

Figure 4.22:	Contour of electric field lines at $V_d = 1$ V under (a) SG and (b) DG operation-mode for a std-GP structure and (c) the corresponding electric field at 1 nm below BOX	84
Figure 4.23:	Normalized maximum transconductance ($g_{m_max_norm}$) where $g_{m_max_norm} = (g_{m_max}/(W/L))$ of UTBB SOI MOSFETs of $L_g = 10$ nm and $W = 1$ μ m at $V_d = 1$ V for SG and DG configurations	85
Figure 4.24:	I_d - V_g curves for UTBB SOI MOSFETs with different GP structures for (a) $T_{si} = 5$ nm and (b) $T_{si} = 12$ nm	88
Figure 4.25:	Impact of different T_{si} on <i>DIBL</i> for UTBB SOI MOSFETs with different GP structures	89
Figure 4.26:	Variations of normalized maximum transconductance ($g_{m_max}/(W/L)$) with different T_{si} as a function of V_g at $V_d = 1$ V for (a) std-GP (b) GP-A and (c) GP-B	93
Figure 4.27:	Impact of different gate dielectric on <i>DIBL</i> as a function of different GP structures under DG operation-mode	96
Figure 4.28:	Two-dimensional (2D) electric field distributions for GP-B structure with $L_g = 10$ nm at $V_g = 1.5$ V and $V_d = 20$ mV for SiO ₂ and HfO ₂	97
Figure 4.29:	Variations of transconductance (g_m) with different high- κ materials as a function of V_g at $V_d = 1$ V for (a) std-GP (b) GP-A and (c) GP-B	99
Figure 4.30:	Variations of g_m with A_v and L_g extracted at various frequencies at $V_g = V_d = 1$ V (Makovejev et al., 2015)	102
Figure 4.31:	g_m/W as a function of A_{vo} for different devices and processes (Valeriya Kilchytska, Makovejev, Md Arshad, Raskin, & Flandre, 2014)	103

Figure 5.1 (a) 3D view of SON MOSFET. The buried pre-etched cavity is smaller in size than the active silicon area and (b) cross-section made along the channel length of a SON MOSFET (Chung, Olbrechts, Södervall, et al., 2007) 108

Figure 5.2 (Left) Cross-section TEM image of high- κ /metal gate MOSFET transistor on SOD substrate with gate length of 200 nm. (Right) Two zones of interest are subjected to HRTEM imaging: gate insulator to top silicon and diamond to top silicon interfaces (projected pictures, respectively on top right and bottom right) (Mazellier et al., 2013) 108

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LIST OF ABBREVIATIONS

1DEG	One-dimensional electron gas
2D	Two-dimensional
2DEG	Two-dimensional electron gas
3D	Three-dimensional
AC	Alternating current
ADG	Asymmetric double-gate
BOX	Buried oxide
CC	Constant current
CMOS	Complementary metal-oxide-semiconductor
DC	Direct current
DG	Double-gate
DIBL	Drain-induced barrier lowering
EI	Electrostatic integrity
ELR	Extrapolation of linear region
ENG	Effective number of gates
EOT	Equivalent oxide thickness
ETSOI	Extremely thin SOI
FBE	Floating body effect
FD	Fully depleted
FD-SOI	Fully-depleted silicon-on-insulator
FinFET	Fin field-effect transistor
FoM	Figure-of-merit
GAA	Gate-all-around
GMLE	Transconductance linear extrapolations
GP	Ground plane
High- κ	High permittivity gate-dielectric
HRTEM	High-resolution transmission electron microscopy
IC	Integrated circuit
ITRS	International Technology Roadmap for Semiconductor
Low- κ	Low permittivity gate-dielectric
MOSFET	Metal-oxide-semiconductor field-effect transistor

NMOS	N-type metal-oxide-semiconductor
PD-SOI	Partially-depleted silicon-on-insulator
PMOS	P-type metal-oxide-semiconductor
QDG	Quasi double-gate
RF	Radio frequency
RM	Ratio method
SCE	Short-channel effects
S/D	Source/drain
SD	Second derivative
SDL	Second derivative logarithmic
SG	Single-gate
SiGe	Silicon germanium
Si-SiO ₂	Silicon-silicon dioxide
SiO ₂	Silicon dioxide
SiN	Silicon nitride
SOD	Silicon-on-diamond
SOI	Silicon-on-insulator
SON	Silicon-on-nothing
SRH	Shockley-Read Hall
SS	Subthreshold swing
TCAD	Technology Computer Aided Design
TEM	Transmission electron microscopy
UTB	Ultra-thin body
UTBB	Ultra-thin body and BOX

LIST OF SYMBOLS

A	Area
A_v	Intrinsic gain
C	Capacitance
C_{gg}	Gate-to-gate capacitance
C_{ox1}	Front gate oxide capacitance
C_{ox2}	Buried oxide capacitance
C_{si}	Silicon film capacitance
E_i	Intrinsic Fermi level
f	Frequency
f_t	Current gain cut-off frequency
g_d	Output conductance
g_m	Transconductance
g_{m_max}	Maximum transconductance
$g_{m_max_norm}$	Normalized maximum transconductance
I	Current
I_d	Drain current
I_d-V_g	Plot of drain current versus gate voltage
I_{d_norm}	Normalized drain current
I_{on}	On-state current
I_{off}	Off-state current
$I-V$	Current voltage
k	Boltzmann constant
κ	Gate dielectric permittivity
$\kappa_{high-\kappa}$	Permittivity of high- κ gate dielectric
κ_{SiO_2}	Permittivity of silicon dioxide gate dielectric
L_{el}	Electrical gate length
L_g	Gate length
n	Body factor
n_i	Intrinsic carrier concentration
N_A	Acceptor doping concentration
N_D	Donor doping concentration

P	Power
q	Charge of an electron
T	Temperature
$t_{\text{high-}\kappa}$	Thickness of high- κ gate dielectric
T_{BOX}	Buried-oxide (BOX) thickness
T_{dep}	Depletion layer thickness
T_{ox}	Gate oxide thickness
$T_{\text{ox_el}}$	Electrical oxide thickness
T_{si}	Silicon-body thickness
V_{bi}	Built-in voltage
V_{d}	Drain voltage
$V_{\text{drain (linear)}}$	Linear drain voltage
$V_{\text{drain(saturation)}}$	Saturation drain voltage
V_{dd}	Supply voltage
V_{g}	Gate voltage
V_{th}	Threshold voltage
$V_{\text{th(linear)}}$	Linear threshold voltage
$V_{\text{th(saturation)}}$	Saturation threshold voltage
V_{sub}	Substrate voltage
W	Width of channel
ϵ	Electric field
ϵ_{ox}	Permittivity of oxide
ϵ_{Si}	Permittivity of silicon
ϵ_{SiO_2}	Permittivity of silicon dioxide
x_{dmax}	Depletion zone extending from the Si-SiO ₂ interface to the maximum depletion width
x_{j}	Junction depth
τ	Gate delay
μ	Mobility
λ	Fitting parameter to take into account the contribution of BOX fringing field
α	Scaling factor
Φ_{F}	Fermi level

Φ_m	Gate workfunction
$\psi_{\text{Horizontal}}$	Horizontal potential
ψ_s	Surface potential
ψ_{Vertical}	Vertical potential

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Simulasi Berangka bagi Konfigurasi Inovatif Satah-Bumi dan Get-Berkembar dalam SOI MOSFETs Badan dan –Oksida Tertanam Nipis

ABSTRAK

Penskalaan transistor membolehkan peningkatan dalam ketumpatan transistor, kelajuan pensuisan dan kekompleksan dengan tiada peningkatan dalam penggunaan kuasa. Walaubagaimanapun, penskalaan transistor MOS yang lazim nampak menuju ke arah akhir pelan tindakan teknologi disebabkan oleh kebolehubahan prestasi yang semakin buruk dan kesan saluran-pendek (*SCEs*). Salah satu pesaing yang dijangka menggantikan seni bina transistor semasa adalah SOI MOSFETs planar badan dan oksida tertanam nipis (UTBB). Kelebihan struktur SOI badan-nipis terletak pada proses planarnya yang mudah yang serasi sepenuhnya dengan aliran CMOS silikon pukat. Dalam kerja kajian ini, perhatian khusus diberikan terhadap prestasi UTBB SOI MOSFETs dengan BOX yang nipis dalam meningkatkan tingkah laku elektrostatik oleh badan-nipis dibandingkan dengan transistor SOI dengan BOX yang tebal (UTB) untuk melanjutkan kebolehskalaan CMOS. Selanjutnya, UTBB dengan seni bina satah bumi (GP) dan konfigurasi get yang berbeza (i.e. get-tunggal (SG) dan get-ganda (DG)) dikaji secara menyeluruh melalui simulasi berangka sebagai calon yang mungkin untuk meneruskan Hukum Moore. Kajian mendalam mengenai angka merit (FoM) digital dan analog/RF dijalankan dalam julat frekuensi yang lebar (dari 0.01 Hz sehingga 100 GHz) dalam hubungan dengan mekanisme operasi peranti. Didapati bahawa pembentukan GP inovatif yang terdiri daripada GP setempat jenis $-p$ dalam substrat di bawah saluran (di sini dirujuk sebagai GP-B dalam tesis) menekan kesan susutan substrat secara efektif dan menunjukkan imuniti yang lebih baik terhadap SCEs daripada pandangan analisis digital. Peningkatan selanjutnya dalam imuniti terhadap SCEs dapat dicapai dengan konfigurasi DG di mana kesan seni bina GP yang berbeza digandakan dibandingkan dengan SG. Walaupun penggunaan konfigurasi DG memberikan prestasi digital yang unggul, nilai frekuensi potongan gandaan intrinsik (f_i) adalah rendah dalam domain analog berbanding SG disebabkan oleh peningkatan kemuatan berparasit get-ke-get (C_{gg}). Oleh itu, pemilihan yang cermat dan keseimbangan diperlukan apabila memilih struktur peranti tertentu di mana hasil yang diperolehi daripada penyelidikan ini menyumbang kepada pengenalpastian seni bina GP dan konfigurasi get (SG atau DG) yang boleh dipakai dalam rekabentuk peranti untuk disesuaikan dengan aplikasi spesifik sama ada digital atau RF.

Numerical Simulations of Innovative Ground Plane (GP) and Double-gate (DG) Configurations in Thin-body and –buried Oxide of SOI MOSFETs

ABSTRACT

The downscaling of transistors enables an increased in transistor density, faster switching speeds and greater complexity with no increase in power consumption. However, the scaling of the conventional planar MOS transistors appears to be reaching the end of the technology roadmap due to worsening performance variability and short-channel effects (SCEs). One of the contenders anticipated to replace the current transistor architecture is planar ultra-thin body and BOX (UTBB) SOI MOSFET. The advantage of the thin-body SOI structure lies in its simple planar process which is fully compatible with the bulk silicon CMOS flow. In this research work, a particular attention is being given to the performance of UTBB SOI MOSFETs with its thin BOX in improving electrostatics behaviour namely of drain-induced barrier lowering (*DIBL*) of the thin-body as compared to thick BOX (UTB) SOI transistors for extending CMOS scalability. Subsequently, UTBB with different ground plane (GP) architectures and gate configurations (i.e. single-gate (SG) vs double-gate (DG)) are extensively studied through numerical simulations as possible candidates for the continuation of Moore's Law. In-depth study of the digital and analog/RF figure-of-merit (FoM) are carried out in a wide range of frequency (from 0.01 Hz to 100 GHz) in correlation with device operation mechanisms. It is discovered that an innovative GP formation made of localized GP of p-type in the substrate underneath the channel (referred herein throughout the thesis as GP-B) effectively suppress substrate depletion effects and shows better immunity against SCEs from the digital analysis viewpoint. Further improvements in the immunity against SCEs can be achieved in DG configurations where the impact of different GP architectures is amplified as compared to SG. Even though the use of DG configurations provides superior digital performance, lower current gain cut-off frequency (f_t) values are produced than SG in the analog domain due to an increase of gate-to-gate capacitances (C_{gg}). Therefore, careful selections and trade-offs are needed when selecting a particular device structure where the results obtained in this research work contribute to the identifications of GP architectures and gate configurations (SG or DG) that can be adopted in device design to suit specific applications of either digital or RF.

CHAPTER 1

INTRODUCTION

1.1 General review of CMOS Technology

1.1.1 Scaling of CMOS Technology to Their Limits

The integrated circuit (IC) technology has followed Moore's Law since 1965 which states that the number of devices integrated double every 18 months. This progression is made possible by continuous miniaturization in feature size of components devices which are integrated – a concept known as device scaling. In detailed, device scaling refers to scaling of various structural parameters of a MOSFET to ensure the device continue to function properly. These include lateral as well as vertical dimensions such as the channel length, the width, the source/drain junction depth (x_j) and the gate oxide thickness (T_{ox}). For proper device scaling, power supply voltages should also be reduced to keep the internal field constant. The first complete scaling scheme known as constant-field scaling was introduced by Dennard et al. (1974) as shown in Table 1.1 and is regarded as the seminal reference in scaling theory for MOSFET integrated circuits. Depending on the variable, the parameter could be multiplied, or divided by α which is a unitless scaling factor. However, as voltage is not usually scaled as fast as the linear dimensions due to subthreshold leakage constraint, additional scaling factor for the electric field (ϵ) is introduced to account for the increased of ϵ and is summarized as 'generalized scaling factor' as shown in Table 1.1.

The scaling of the transistor's feature size leads to an increased speed and improved density (smaller areas for devices and circuits).

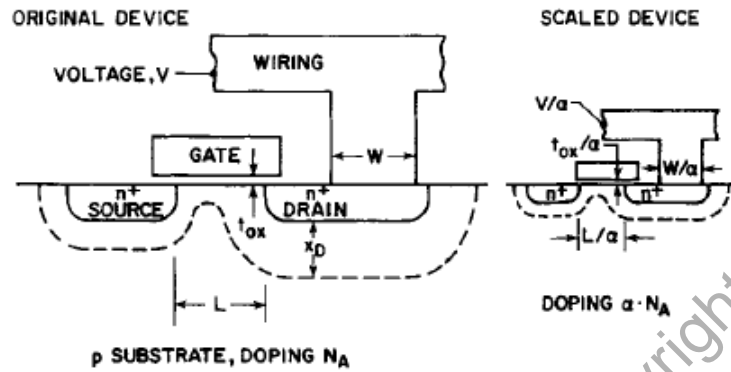


Figure 1.1: Principles of MOSFET constant-field scaling (Davari, Dennard, & Shahidi, 1995)

Table 1.1: The classical scaling trends

Parameters	Constant-field scaling (Dennard et al., 1974)	Generalized scaling factor (Baccarani, Wordeman, & Dennard, 1984)
Physical dimensions (L_g, W, T_{ox}, x_j)	$1/\alpha$	$1/\alpha$
Electric field (ϵ)	1	ϵ
Body doping concentration (N_A)	α	ϵ/α
Supply voltage (V_{dd})	$1/\alpha$	ϵ/α
Transistor current (I)	$1/\alpha$	ϵ/α
Capacitance ($C = \epsilon_{ox} A / T_{ox}$)	$1/\alpha$	$1/\alpha$
Area (A)	$1/\alpha^2$	$1/\alpha^2$
Gate delay ($\tau \sim C V_{dd} / I$)	$1/\alpha$	ϵ/α
Power dissipation ($P \sim I V_{dd}$)	$1/\alpha^2$	ϵ^2/α^2
Power density (P/A)	1	ϵ^2

1.1.2 Scaling Challenges

The classical scaling technique of MOSFET was followed successfully until 90 nm transistor generation (M. Bohr, 2008, 2009; Kuhn, 2009) (The last CMOS generation where the downscaling of transistor to make it smaller is adequate to improve the transistor's performance is of the 130 nm transistor generation). In the following generation, it is then recognized that simple scaling of bulk MOSFETs i.e. increasing the doping in the channel and reducing the silicon thickness is no longer valid as a result of rapidly increasing random variability and poor short channel immunity. With the shrinking of the transistor gate length (L_g), the lateral electric fields at the source and drain can penetrate into the channel, causing reduction in barrier height of source/body junction. This will lead to an increase in short-channel effects (SCEs).

SCEs arise when the close proximity between the source and the drain causes the gate to lose control of the potential distribution and the flow of current in the channel region. With shorter L_g , the depletion regions of high electric fields associated with the source and drain regions started to interact with each other, causing direct carrier transport between the source and drain. This reduces control of the gate over the channel and in turn, rise in off-state current (I_{off}) and lower threshold voltage (V_{th}) are observed. In conventional MOSFET, decreasing L_g has been accompanied by the decreased in gate oxide thickness (T_{ox}) and the source/drain junction depth (x_j). However, an increased in gate leakage current caused by tunnelling through the very thin oxide (~ 2 nm) has put the limit to oxide scaling. It is then proposed that higher

permittivity (high- κ) materials to be used as gate dielectrics. The use of high- κ materials enables the use of a physically thicker oxide while reducing its equivalent oxide thickness (EOT) which prevents gate tunnelling. However, further downscaling into the sub-10 nm regime can lead to a huge direct tunnelling between source and drain which degrades SS and increase the I_{off} and power dissipation. Figure 1.2 shows the limit of scaling (Ahmad & Schuegraf, 2011). In order to be able to continue device scaling down to 20 nm and beyond, the need to explore both alternative materials and alternative device architectures is indispensable.

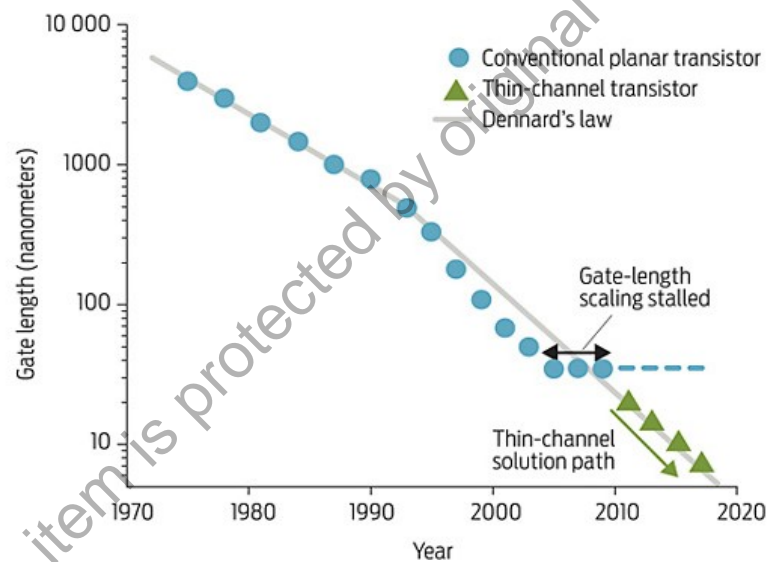


Figure 1.2: Limits of downscaling (Ahmad & Schuegraf, 2011)

1.1.3 Advanced CMOS Technology

The strain engineering has been a striking method for enhancing the carrier mobility of the CMOS technology at 90-nm node in 2003 and beyond (Gehres et al., 2006; Ghani et al., 2003; Thompson et al., 2004). Silicon germanium (SiGe) was selectively deposited on source-drain regions in P-type metal-oxide-semiconductor