NUMERICAL SIMULATIONS OF INNOVATIVE GROUND PLANE AND DOUBLE-GATE CONFIGURATIONS IN THIN-BODY AND – BURIED OXIDE OF SOI MOSFETs

by

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LIST OF ABBREVIATIONS

1DEG	One-dimensional electron gas
2D	Two-dimensional
2DEG	Two-dimensional electron gas
3D	Three-dimensional
AC	Alternating current
ADG	Asymmetric double-gate
BOX	Buried oxide
CC	Constant current
CMOS	Complementary metal-oxide-semiconductor
DC	Direct current
DG	Double-gate
DIBL	Drain-induced barrier lowering
EI	Electrostatic integrity
ELR	Extrapolation of linear region
ENG	Effective number of gates
EOT	Equivalent oxide thickness
ETSOI	Extremely thin SOI
FBE	Floating body effect
FD	Fully depleted
FD-SOI	Fully-depleted silicon-on-insulator
FinFET	Fin field-effect transistor
FoM	Figure-of-merit
GAA	Gate-all-around
GMLE	Transconductance linear extrapolations
GP	Ground plane
High-κ	High permittivity gate-dielectric
HRTEM	High-resolution transmission electron microscopy
IC	Integrated circuit
ITRS	International Technology Roadmap for Semiconductor
Low-κ	Low permittivity gate-dielectric
MOSFET	Metal-oxide-semiconductor field-effect transistor

NMOS	N-type metal-oxide-semiconductor
PD-SOI	Partially-depleted silicon-on-insulator
PMOS	P-type metal-oxide-semiconductor
QDG	Quasi double-gate
RF	Radio frequency
RM	Ratio method
SCE	Short-channel effects
S/D	Source/drain
SD	Second derivative
SDL	Second derivative logarithmic
SG	Single-gate
SiGe	Silicon germanium
Si-SiO_2	Silicon-silicon dioxide
SiO_2	Silicon dioxide
SiN	Silicon nitride
SOD	Silicon-on-diamond
SOI	Silicon-on-insulator
SON	Silicon-on-nothing
SRH	Shockley-Read Hall
SS	Subthreshold swing
TCAD	Technology Computer Aided Design
TEM	Transmission electron microscopy
UTB	Ultra-thin body
UTBB	Ultra-thin body and BOX

LIST OF SYMBOLS

A	Area
A_v	Intrinsic gain
C	Capacitance
C_{gg}	Gate-to-gate capacitance
C_{ox1}	Front gate oxide capacitance
C_{ox2}	Buried oxide capacitance
C_{si}	Silicon film capacitance
E_i	Intrinsic Fermi level
f	Frequency
f_t	Current gain cut-off frequency
g_d	Output conductance
g_m	Transconductance
g_{m_max}	Maximum transconductance
$g_{m\_max\_norm}$	Normalized maximum transconductance
I	Current
I_d	Drain current
I_d-V_g	Plot of drain current versus gate voltage
I_{d_norm}	Normalized drain current
I_{on}	On-state current
I_{off}	Off-state current
I-V	Current voltage
k	Boltzmann constant
κ	Gate dielectric permittivity
$\kappa_{high\text{-}\kappa}$	Permittivity of high-κ gate dielectric
κ_{SiO2}	Permittivity of silicon dioxide gate dielectric
L_{el}	Electrical gate length
L_g	Gate length
n	Body factor
n_i	Intrinsic carrier concentration
N_A	Acceptor doping concentration
N_D	Donor doping concentration

P	Power
q	Charge of an electron
T	Temperature
$t_{\text{high-}\kappa}$	Thickness of high-κ gate dielectric
T_{BOX}	Buried-oxide (BOX) thickness
T_{dep}	Depletion layer thickness
T_{ox}	Gate oxide thickness
$T_{\text{ox\_el}}$	Electrical oxide thickness
T_{si}	Silicon-body thickness
V_{bi}	Built-in voltage
V_{d}	Drain voltage
$V_{\text{drain (llinear)}}$	Linear drain voltage
$V_{\text{drain(saturation)}}$	Saturation drain voltage
V_{dd}	Supply voltage
V_{g}	Gate voltage
V_{th}	Threshold voltage
$V_{\text{th(linear)}}$	Linear threshold voltage
$V_{\text{th(saturation)}}$	Saturation threshold voltage
V_{sub}	Substrate voltage
W	Width of channel
$\in$	Electric field
ε_{ox}	Permittivity of oxide
ε_{Si}	Permittivity of silicon
$\varepsilon_{\text{SiO2}}$	Permittivity of silicon dioxide
x_{dmax}	Depletion zone extending from the Si-SiO_2 interface to the maximum depletion width
x_{j}	Junction depth
τ	Gate delay
μ	Mobility
λ	Fitting parameter to take into account the contribution of BOX fringing field
α	Scaling factor
Φ_{F}	Fermi level

Φ_m	Gate workfunction
$\psi_{Horizontal}$	Horizontal potential
ψ_s	Surface potential
$\psi_{Vertical}$	Vertical potential

Simulasi Berangka bagi Konfigurasi Inovatif Satah-Bumi dan Get-Berkembar dalam SOI MOSFETs Badan dan –Oksida Tertanam Nipis

ABSTRAK

Penskalaan transistor membolehkan peningkatan dalam ketumpatan transistor, kelajuan pensuisan dan kekompleksan dengan tiada peningkatan dalam penggunaan kuasa. Walaubagaimanapun, penskalaan transistor MOS yang lazim nampak menuju ke arah akhir pelan tindakan teknologi disebabkan oleh kebolehubahan prestasi yang semakin buruk dan kesan saluran-pendek (*SCEs*). Salah satu pesaing yang dijangka menggantikan seni bina transistor semasa adalah SOI MOSFETs planar badan dan oksida tertanam nipis (UTBB). Kelebihan struktur SOI badan-nipis terletak pada proses planarnya yang mudah yang serasi sepenuhnya dengan aliran CMOS silikon pukal. Dalam kerja kajian ini, perhatian khusus diberikan terhadap prestasi UTBB SOI MOSFETs dengan BOX yang nipis dalam meningkatkan tingkah laku elektrostatik oleh badan-nipis dibandingkan dengan transistor SOI dengan BOX yang tebal (UTB) untuk melanjutkan kebolehskalaan CMOS. Selanjutnya, UTBB dengan seni bina satah bumi (GP) dan konfigurasi get yang berbeza (i.e. get-tunggal (SG) dan get-ganda (DG)) dikaji secara menyeluruh melalui simulasi berangka sebagai calon yang mungkin untuk meneruskan Hukum Moore. Kajian mendalam mengenai angka merit (FoM) digital dan analog/RF dijalankan dalam julat frekuensi yang lebar (dari 0.01 Hz sehingga 100 GHz) dalam hubungan dengan mekanisme operasi peranti. Didapati bahawa pembentukan GP inovatif yang terdiri daripada GP setempat jenis –p dalam substrat di bawah saluran (di sini dirujuk sebagai GP-B dalam tesis) menekan kesan susutan substrat secara efektif dan menunjukkan imuniti yang lebih baik terhadap SCEs daripada pandangan analisis digital. Peningkatan selanjutnya dalam imuniti terhadap SCEs dapat dicapai dengan konfigurasi DG di mana kesan seni bina GP yang berbeza digandakan dibandingkan dengan SG. Walaupun penggunaan konfigurasi DG memberikan prestasi digital yang unggul, nilai frekuensi potongan gandaan intrinsik (f_t) adalah rendah dalam domain analog berbanding SG disebabkan oleh peningkatan kemuatan berparasit get-ke-get (C_{gg}). Oleh itu, pemilihan yang cermat dan keseimbangan diperlukan apabila memilih struktur peranti tertentu di mana hasil yang diperolehi daripada penyelidikan ini menyumbang kepada pengenalpastian seni bina GP dan konfigurasi get (SG atau DG) yang boleh dipakai dalam rekabentuk peranti untuk disesuaikan dengan aplikasi spesifik sama ada digital atau RF.

Numerical Simulations of Innovative Ground Plane (GP) and Double-gate (DG) Configurations in Thin-body and –buried Oxide of SOI MOSFETs

ABSTRACT

The downscaling of transistors enables an increased in transistor density, faster switching speeds and greater complexity with no increase in power consumption. However, the scaling of the conventional planar MOS transistors appears to be reaching the end of the technology roadmap due to worsening performance variability and short-channel effects (SCEs). One of the contenders anticipated to replace the current transistor architecture is planar ultra-thin body and BOX (UTBB) SOI MOSFET. The advantage of the thin-body SOI structure lies in its simple planar process which is fully compatible with the bulk silicon CMOS flow. In this research work, a particular attention is being given to the performance of UTBB SOI MOSFETs with its thin BOX in improving electrostatics behaviour namely of drain-induced barrier lowering (*DIBL*) of the thin-body as compared to thick BOX (UTB) SOI transistors for extending CMOS scalability. Subsequently, UTBB with different ground plane (GP) architectures and gate configurations (i.e. single-gate (SG) vs double-gate (DG)) are extensively studied through numerical simulations as possible candidates for the continuation of Moore's Law. In-depth study of the digital and analog/RF figure-of-merit (FoM) are carried out in a wide range of frequency (from 0.01 Hz to 100 GHz) in correlation with device operation mechanisms. It is discovered that an innovative GP formation made of localized GP of p-type in the substrate underneath the channel (referred herein throughout the thesis as GP-B) effectively suppress substrate depletion effects and shows better immunity against SCEs from the digital analysis viewpoint. Further improvements in the immunity against SCEs can be achieved in DG configurations where the impact of different GP architectures is amplified as compared to SG. Even though the use of DG configurations provides superior digital performance, lower current gain cut-off frequency (f_t) values are produced than SG in the analog domain due to an increase of gate-to-gate capacitances (C_{gg}). Therefore, careful selections and trade-offs are needed when selecting a particular device structure where the results obtained in this research work contribute to the identifications of GP architectures and gate configurations (SG or DG) that can be adopted in device design to suit specific applications of either digital or RF.

CHAPTER 1

INTRODUCTION

1.1 General review of CMOS Technology

1.1.1 Scaling of CMOS Technology to Their Limits

The integrated circuit (IC) technology has followed Moore's Law since 1965 which states that the number of devices integrated double every 18 months. This progression is made possible by continuous miniaturization in feature size of components devices which are integrated - a concept known as device scaling. In detailed, device scaling refers to scaling of various structural parameters of a MOSFET to ensure the device continue to function properly. These include lateral as well as vertical dimensions such as the channel length, the width, the source/drain junction depth (x_j) and the gate oxide thickness (T_{ox}). For proper device scaling, power supply voltages should also be reduced to keep the internal field constant. The first complete scaling scheme known as constant-field scaling was introduced by Dennard et al. (1974) as shown in Table 1.1 and is regarded as the seminal reference in scaling theory for MOSFET integrated circuits. Depending on the variable, the parameter could be multiplied, or divided by α which is a unitless scaling factor. However, as voltage is not usually scaled as fast as the linear dimensions due to subthreshold leakage constraint, additional scaling factor for the electric field (ϵ) is introduced to account for the increased of ϵ and is summarized as 'generalized scaling factor' as shown in Table 1.1.

The scaling of the transistor's feature size leads to an increased speed and improved density (smaller areas for devices and circuits).

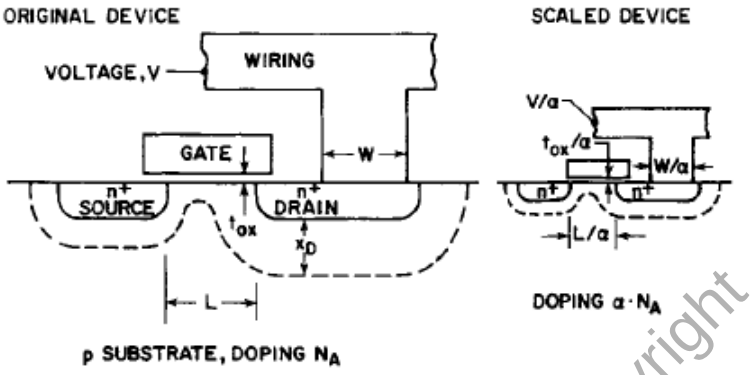

Figure 1.1: Principles of MOSFET constant-field scaling (Davari, Dennard, & Shahidi, 1995)

Table 1.1: The classical scaling trends

Parameters	Constant-field scaling (Dennard et al., 1974)	Generalized scaling factor (Baccarani, Wordeman, & Dennard, 1984)
Physical dimensions (L_g,W, $T_{ox,}$ x_j)	$1/\alpha$	$1/\alpha$
Electric field (ϵ)	1	ϵ
Body doping concentration (N_A)	α	ϵ/α
Supply voltage (V_{dd})	$1/\alpha$	ϵ/α
Transistor current (I)	$1/\alpha$	ϵ/α
Capacitance ($C= \varepsilon_{ox}A/ T_{ox}$)	$1/\alpha$	$1/\alpha$
Area (A)	$1/ \alpha^2$	$1/ \alpha^2$
Gate delay ($\tau \sim C V_{dd} /I$)	$1/\alpha$	ϵ/α
Power dissipation ($P \sim IV_{dd}$)	$1/ \alpha^2$	ϵ^2/α^2
Power density (P/A)	1	ϵ^2

1.1.2 Scaling Challenges

The classical scaling technique of MOSFET was followed successfully until 90 nm transistor generation (M. Bohr, 2008, 2009; Kuhn, 2009) (The last CMOS generation where the downscaling of transistor to make it smaller is adequate to improve the transistor's performance is of the 130 nm transistor generation). In the following generation, it is then recognized that simple scaling of bulk MOSFETs i.e. increasing the doping in the channel and reducing the silicon thickness is no longer valid as a result of rapidly increasing random variability and poor short channel immunity. With the shrinking of the transistor gate length (L_g), the lateral electric fields at the source and drain can penetrate into the channel, causing reduction in barrier height of source/body junction. This will lead to an increase in short-channel effects (SCEs).

SCEs arise when the close proximity between the source and the drain causes the gate to lose control of the potential distribution and the flow of current in the channel region. With shorter L_g, the depletion regions of high electric fields associated with the source and drain regions started to interact with each other, causing direct carrier transport between the source and drain. This reduces control of the gate over the channel and in turn, rise in off-state current (I_{off}) and lower threshold voltage (V_{th}) are observed. In conventional MOSFET, decreasing L_g has been accompanied by the decreased in gate oxide thickness (T_{ox}) and the source/drain junction depth (x_j). However, an increased in gate leakage current caused by tunnelling through the very thin oxide (~2 nm) has put the limit to oxide scaling. It is then proposed that higher

permittivity (high-κ) materials to be used as gate dielectrics. The use of high-κ materials enables the use of a physically thicker oxide while reducing its equivalent oxide thickness (*EOT*) which prevents gate tunnelling. However, further downscaling into the sub-10 nm regime can lead to a huge direct tunnelling between source and drain which degrades *SS* and increase the I_{off} and power dissipation. Figure 1.2 shows the limit of scaling (Ahmad & Schuegraf, 2011). In order to be able to continue device scaling down to 20 nm and beyond, the need to explore both alternative materials and alternative device architectures is indispensable.

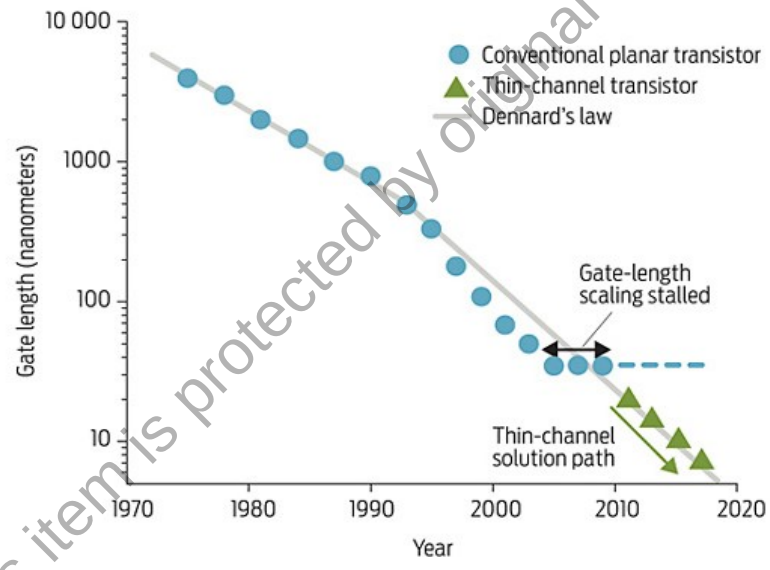

Figure 1.2: Limits of downscaling (Ahmad & Schuegraf, 2011)

1.1.3 Advanced CMOS Technology

The strain engineering has been a striking method for enhancing the carrier mobility of the CMOS technology at 90-nm node in 2003 and beyond (Gehres et al., 2006; Ghani et al., 2003; Thompson et al., 2004). Silicon germanium (SiGe) was selectively deposited on source-drain regions in P-type metal-oxide-semiconductor