



**A NOVEL ENERGY EFFICIENT OF NETWORK-
ON-CHIP (NoC) ARCHITECTURE FOR SYSTEM-
ON-CHIP (SoC)**

by

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LIST OF ABBREVIATIONS

ASIC	Application Specific Integrated Circuit
AXI	Advanced Extensible Interface
BFT	Butterfly Fat Tree
CBHR	Cluster Based Hierarchical Routing
CMOS	Complementary Metal Oxide Semiconductor
CMPs	Chip Multiprocessors
CMOS	Complementary Metal Oxide Semiconductor
CNOC	Clustered NoC
CSA	Clustering-based Simulated Annealing
CTG	Communication Task Graph
Cluster-TG	Cluster-based noC Topology Generation
DTL	Diode Transistor Logic
ECC	Error Correcting Coding
FLIT	Flow Control Digit
FPGA	Field Programmable Gate Array
HoL	Head of Line
IC	Integrated Circuit
IP	Intellectual Property
NI	Network Interface
NoC	Network on Chip
OSI	Open System Interface
PE	Processing Element
PLP	Power Latency Product
QoS	Quality of Service
RAM	Random Access Memory
RTL	Register Transfer Language
SoC	System on Chip
SPIN	Scalable Programmable Integrated Network
TTL	Time to Live
VC	Virtual Channel
XFA	XY Fully Adaptive

Satu Pembaharuan Tenaga Efisien Seni Bina Rangkaian di Atas Cip (NoC) Untuk Sistem di Atas Cip (SoC)

ABSTRAK

Memandangkan bilangan integrasi harta intelektual (IP) pada cip meningkat, cabaran yang serius akan dihadapi dalam mencapai prestasi dan kuasa yang diperlukan untuk memenuhi kekangan cip pada masa depan. Penambahan rangkaian pintar pada cip itu menambah penggunaan kuasa rangkaian di atas cip (NoC), dengan itu sistem di atas cip (SoCs) diperlukan untuk memberikan prestasi tinggi dan infrastruktur sambungan penggunaan kuasa yang rendah kepada sejumlah besar teras. Untuk mencapai matlamat tersebut, penyelidikan ini memberi tumpuan kepada cadangan cara menggunakan rangkaian saling sambung yang sedia ada untuk menyediakan prestasi yang lebih baik, kawasan output, dan kuasa efisien NoC dengan mengoptimumkan seni bina saling sambung. Untuk menyelesaikan masalah yang dihadapi dengan rangkaian berskala besar, reka bentuk penjimatan kuasa penggugusan, segmen-ketersambungan, dan strategi sekatan berguna untuk aplikasi pelbagai homogen yang perlu dilaksanakan selari dan dipetakan pada rangkaian besar. Teknik ini menurunkan bilangan pautan dan mengurangkan jarak purata rangkaian, yang membantu dalam mencapai penggunaan kuasa yang rendah. Topologi boleh mengelompokkan, membahagikan, dan menyekat sifat yang sama ke dalam kumpulan yang sama. Nod dalam kumpulan yang sama sangat banyak disambungkan, manakala nod dalam kumpulan yang berlainan jarang tersambung. Objektif penyelidikan adalah untuk mencari tahap topologi yang paling cekap dan pertunjukan yang paling tinggi berdasarkan penggugusan, segmen-ketersambungan, dan strategi sekatan. Pada masa yang sama meminimumkan penalti prestasi dengan memohon mod tidur, mod tunggu sedia, dan mod hibernasi berdasarkan aplikasi masa jalan, kerana aplikasi berbeza menunjukkan keperluan saiz yang berbeza dalam penggugusan, segmen, dan sekatan. Dengan cekap mengendalikan sambungan penggugusan, segmen-ketersambungan, dan teknik sekatan, hasil eksperimen menunjukkan bahawa teknik mencapai 9.39% ~ 71.89% penjimatan kuasa, sehingga 0.97% ~ 54.76% penjimatan kawasan output, mengurangkan purata kependaman rangkaian sehingga 9.81% ~ 76.26%, dan sehingga 6.65% ~ 78.96% penjimatan kuasa kependaman hasil darab (PLP) berbanding dengan topologi yang sedia ada. Kesimpulannya, hasilnya menunjukkan jika mematikan nod dari penggugusan, segmen, dan sekatan topologi akan mengurangkan penggunaan kependaman dan kuasa. Hasilnya juga menunjukkan pentingnya pengoptimuman kuasa dan kependaman penting dalam reka bentuk NoC.

A Novel Energy Efficient of Network-on-Chip (NoC) Architecture for System-on-Chip (SoC)

ABSTRACT

As the number of intellectual property (IP) integrated into a chip increases, this can present serious challenges to achieving the performance and power needed for satisfying the constraint on future chip. The addition of the intelligent networking on the chip adds to the power consumption of network-on-chip (NoC). Thus, system-on-chip (SoCs) is required to be capable of delivering high performance and consuming low power, of the interconnection infrastructure to large number of cores. This research aims to focus on proposing ways to use current available network interconnection modal to provide NoC of better performance, smaller total area, and higher power efficiency, by optimizing interconnection architecture. In order to solve the problem encountered with large scale network, a design of power saving clustering, segmentation-connectivity, and partition technique is useful for multiple homogeneous applications which need to be executed in parallel and mapped on a large network. This technique reduces the number of link and lowers the average distance of a network, which help in achieving low power consumption. Topology can be clustering, segmenting, and partitioning the cores of similar characteristic into the same group. The nodes in the same group are highly connected, while the nodes in different group are sparsely connected. The objective of research is to search for the most power efficient and performance aware topologies based on clustering, segmentation-connectivity, and partition strategy. At the same time, this research minimizes performance penalty by applying sleep mode, standby mode, and hibernation mode based on different runtime application. This is crucial as different application has different requirement of logical cluster, segment, and partition size. By efficiently handling the connection of clustering, segmentation-connectivity, and partition technique, the experimental results show that these techniques achieve up to 9.39% ~ 71.89% power saving, up to 0.97% ~ 53.59% area saving; reduce average network latency up to 9.81% ~ 76.26%; and up to 6.65% ~ 78.96% power latency product (PLP) saving as compared to traditional topology. In the end, the results show that turning 'off' the nodes of the cluster, segment, and partition topologies reduce latency and power consumption. The results also indicate the importance of power and latency co-optimization in NoC design.

CHAPTER 1 : INTRODUCTION

1.1 Overview

The term system-on-chip (SoC) has come to be used to refer to a small chip that contains all components of a complex system. Due to the increasing number of processing element (PE) on a chip, the size of the transistors has reached the physical processor limitation (Hollstein, Peng, Ubar, & Glesner, 2001), particularly for traditional bus-based and point-to-point architectures in SoC. Under this circumstance, the SoC's diameter and complexity of wired connection is increasing. This becomes the leading cause of problem of bandwidth, signal integrity, and power consumption (Malik & Iqbal, 2011). Similarly, as the number of core increases, the impact on power consumption increases on buses system. Hence, further investigations need to be undertaken in power saving mechanism in network-on-chip (NoC) with appropriate architecture, so as to minimize the power consumption and reduce the effect on heat dissipation.

On-chip interconnection network has been proposed as a solution to the problem encountered in bus and point-to-point network (Agarwal, 2009). However, the design of on-chip communication architecture involves many complicated designs, such as interconnection topology, routing algorithm, switching technique, deadlock detection, and flow control mechanism. On-chip interconnection network provides advantages such as lower latency, higher throughput, lower power consumption, reusability, and scalability (Elisabete & Duarte, 2015). Recently, however, the size of the NoC architecture has been increasing and communication between cores becomes complicated.

To meet the challenges, network interconnection plays an important role in NoC when the number of processing element increases since it highly affects the overall network performance, cost, and power consumption. The size of topology is proportional to the total power consumption and latency (Phing, Mohd Warip, Ehkan, Zulkefli, & Ahmad, 2018). This research focuses on designing the interconnection network architecture of on-chip communication system elements and optimizing the design according to various design objective and constraint. In this research, clustering, segmentation-link, partition strategy is being designed. Besides that, sleep mode, standby mode, hibernation mode mechanism employing clustering, segmentation-connectivity, and partition technique on different NoC metric is being proposed to improve the performance of NoC.

1.2 Problem Statement

To overcome the drawback of system-on-chip (SoC), network-on-chip (NoC) has been proposed as a viable solution. According to Moore's law, the number of transistor per square inch on integrated circuit (IC) that will be integrated into SoC is growing doubled every year since their invention (ITRS, 2015). So, the design of a NoC with low latency, low power consumption, and high throughput system is needed in future. By shrinking the size of transistor down to nano-scale drastically increases the proportion of the static power consumption (Farrokhbakht, Kamali, & Hessabi, 2017). Therefore, high power consumption, as well as high probability of idleness in NoC routers and links, motivate us to focus on reducing static power in on-chip routers and links.