

DESIGN OF SUBSYSTEMS FOR MULTIBAND
WIRELESS TRANSCEIVER

ARJUNA BIN MARZUKI

UNIVERSITI MALAYSIA PERLIS
2010

© This item is protected by original copyright



**DESIGN OF SUBSYSTEMS FOR MULTIBAND
WIRELESS TRANSCEIVER**

by

**ARJUNA BIN MARZUKI
(0640110116)**

**A thesis submitted
In fulfilment of the requirements for the degree of
Doctor of Philosophy**

**School of Microelectronic Engineering
UNIVERSITI MALAYSIA PERLIS**

2010

ACKNOWLEDGEMENTS

First of all I would like to thank Professor Ali Yeon Md. Shakaff and Profesor Madya Zaliman Sauli for their guidance and insight in seeing this thesis through. I would also like to thank certain people in my last and current employment for their valuable assistance especially with their skills in RF measurement techniques.

Thank to School of Microelectronic Engineering, the dean and the administration staffs in supporting my work.

Next I would like to thank my friends, who support me throughout this work. These people are my former colleagues in Avago Technologies; Zulfa, on helping the LNA and MPA development and C-Rad Technologies: Radzi, on moral support.

Thank to my student, Khor Teng Teng in helping me in the simulation of the CMOS VCOs and switch.

I would also like to thank the support and acknowledge the support of Telekom R&D Malaysia Sdn. Bhd. (Project number R05-0607-0, lead by Dr. Ahmad Ismat Abdul Rahim) and Agilent Technologies in the fabrication and measurement of the design.

Next I would like to thank Universiti Sains Malaysia, School of Electrical and Electronic Engineering, my current employer, especially the dean, the administration staffs and colleagues for supporting this endeavor.

Lastly, I would like to thank to my beloved wife and daughter, my parents and brothers for their full support throughout the years. I sincerely dedicated this work to my late brother who has been a very good brother throughout his life. I pray to Almighty for forgiveness and mercy for my humble and simple brother.

TABLE OF CONTENTS

	Page
DECLARATION	ii
ACKNOWLEDGEMENTS	iii
TABLE OF CONTENTS	iv
LIST OF TABLES	x
LIST OF FIGURES	xii
LIST OF SYMBOLS	xx
LIST OF ABBREVIATION	xxvii
LIST OF APPENDICES	xxx
LIST OF ACCEPTED PUBLICATIONS	xxxii
ABSTRAK	xxxiii
ABSTRACT	xxxiv

CHAPTER ONE : INTRODUCTION

1.0	Overview	1
1.1	Motivation	1
1.2	Problem Statement	2
1.3	Objectives	3
1.4	Contribution	3
1.5	Organization of the Thesis	4

CHAPTER TWO : DESIGN CONSTRAINTS OVERVIEW OF HIGH FREQUENCY INTEGRATED CIRCUITS

2.0	Introduction	6
2.1	Receiver Types	9
	2.1.1 Superheterodyne Receiver	9
	2.1.2 Direct-Conversion Receiver(DCR)	11
	2.1.3 Low-IF Receiver	14
	2.1.4 Wide-band IF Receiver	16
2.2	Issues in Receiver Topologies	17

2.2.1	Flicker Noise	17
2.2.2	Even-Order Distortion	18
2.2.3	LO Leakage	19
2.3	Comparison on the Receiver Architectures	20
2.4	I/Q Demodulator	23
2.4.1	Mixer Theory	25
2.4.2	Oscillator	31
2.4.2.1	Tank Circuit	32
2.4.3	Voltage Reference Circuit	33
2.4.4	Current Reference Circuit	34
2.4.5	Frequency Divider	36
2.4.5.1	Analog Frequency Divider	36
2.4.5.2	Digital Frequency Divider	37
2.4.5.2.1	Synchronous and Asynchronous	38
2.4.5.3	Divide by 2 Circuit	38
2.5	Design Flow	39
2.6	MOSFET as a Switch	41
2.6.1	NMOS Switch	41
2.6.2	Transmission Gate	43
2.6.3	Charge Injection	44
2.6.4	NMOS Switch-Design Issues and Discussion	45
2.7	Shunt Feedback Amplifier	47
2.7.1	Shunt Feedback S-Parameter Analysis	48
2.8	Summary	52

CHAPTER THREE : DESIGN METHODOLOGY

3.0	Introduction	53
3.1	PACB	53
3.2	LNA, MPA and Broadband Amplifier Circuits Theory	56
3.2.1	Low Noise Amplifiers	57
3.2.1.1	High Frequency Core Circuit	57
3.2.1.2	High Frequency Core Circuit S-Parameter Analysis	58
3.2.1.2	LNA Design	59
3.2.2	Medium Power Amplifiers	59

3.2.3	Broadband Amplifier	60
3.3	Multiband Demodulator	63
3.3.1	The I/Q Mixer Design	63
3.3.1.1	Voltage Gain	64
3.3.1.2	Mixer Noise	65
3.3.1.3	Linearity	65
3.3.2	The LO-Divider Design	67
3.3.2.1	Master Slave D Flip Flop (MSDFF) Design (divide-by-2)	68
3.3.2.2	MSDFFs (Tied Collectors)	69
3.3.3	Clock Buffer Amplifier Design	70
3.3.4	VCO Buffer Amplifier Design	71
3.3.5	VCS Circuit Design	73
3.3.5.1	VCS Design Theories	73
3.4	Variable Signal Generator	79
3.4.1	Active Oscillators Design Methodology	79
3.4.2	Switch-Series Shunt Topology	81
3.4.3	Oscillator Design – Cross-coupled LC oscillator	82
3.4.4	Design Issues and Discussion	84
3.5	Summary	86

CHAPTER FOUR: LOW NOISE AMPLIFIER, MEDIUM POWER AMPLIFIER AND BROADBAND AMPLIFIER

4.0	Introduction	87
4.1	Transistor Characterization	88
4.1.1	Experimental	88
4.2	Core Circuit Design	92
4.2.1	Parasitic Aware in the Core Circuit	92
4.3	LNA Design	93
4.4	Medium Power Amplifier Design	96
4.5	Broadband Amplifier Design	98
4.5.1	Transistor Size Determination	98
4.6	Summary	103

CHAPTER FIVE: MULTIBAND DEMODULATOR AND VARIABLE SIGNAL GENERATOR

5.0	Introduction	104
5.1	Multiband Demodulator	105
5.1.1	The I/Q Mixer Design	106
5.1.1.1	Voltage Gain	107
5.1.1.2	The Mixer Noise	108
5.1.1.3	The Linearity	108
5.1.2	LO Divider Design	109
5.1.2.1	Negative Resistance Circuit Design	111
5.1.2.2	Master Slave D Flip Flop (MSDFF) Design	112
5.1.2.3	MSDFFs (Tied Collectors) Master Slave D Flip Flop (MSDFF) design	114
5.1.2.4	Clock Buffer Amplifier Design	115
5.1.2.5	VCO Buffer Amplifier Design	116
5.1.3	Control and Bias Circuits Design	117
5.1.3.1	Control Circuit Design	117
5.1.3.2	VCS Circuit Design	120
5.1.4	Input Shifter	121
5.2	Variable Signal Generator	123
5.2.1	Oscillator Design- Cross-coupled LC oscillator	123
5.2.1.1	Calculation	124
5.2.2	Control Signal	126
5.2.3	Biasing Circuit	127
5.2.4	Output Buffer	128
5.3	Summary	129

CHAPTER SIX : RESULTS OF LNA, MPA, BROADBAND AMPLIFIER, MULTIBAND DEMODULATOR AND VARIABLE SIGNAL GENERATOR

6.0	Introduction	130
6.1	Simulation Results	130
6.1.1	Core Circuit	130

6.1.2	LNA	131
6.1.3	MPA	133
6.1.4	Broadband Amplifier	134
6.1.5	Variable Signal Generator	138
6.1.5.1	Simulation Result of Series-Shunt NMOS Switch	139
6.1.5.2	Simulation Result of Cross-Coupled LC Oscillators	140
6.1.5.3	Simulation Result of Variable Signal Generator	143
6.1.5.3.1	Integration of Single Oscillator and Switch	143
6.1.5.3.2	Integration of Three Oscillators	147
6.1.6	Simulation Results of Multiband Demodulator	153
6.1.6.1	Mixer Simulation Results	153
6.1.6.2	LO-Divider Simulation Results	155
6.1.6.3	Buffer Amplifiers Simulation Results	159
6.1.6.4	Control and Bias Circuits Simulation Results	161
6.1.6.5	The I/Q Demodulator Simulation Results	165
6.1.6.6	Post Layout Simulation	170
6.2	Experimental Results	172
6.2.1	Core Circuit	172
6.2.2	LNA	174
6.2.3	MPA	177
6.2.4	Multiband Demodulator	180
6.2.4.1	Introduction	180
6.2.4.2	Output signal	180
6.2.4.3	VCO	181
6.2.4.4	I and Q Gain Imbalance	182
6.2.4.5	I and Q Phase Imbalance	183
6.2.4.6	Error Vector Magnitude	184
6.2.4.7	Discussion	185

CHAPTER SEVEN : CONCLUSIONS AND FUTURE WORK

7.0	Conclusions	187
7.1	Future Work	190

REFERENCES	191
APPENDICES	201
Appendix A1 W-CDMA Receiver Specification	202
Appendix A2 I/Q Demodulator Specification	206
Appendix A3 High Frequency Core Circuit Analysis	210
Appendix A4 Ideal Fully Balanced Mixer	215
Appendix A5 Differential Amplifier (diffamp)-RF core of Mixer	218
Appendix A6 Layout Diagram of I/Q Demodulator	229

© This item is protected by original copyright

LIST OF TABLES

Table	Page
2.1 Comparison on the Capabilities of the Different Receiver Architectures (Pärssinen, 2001)	21
2.2 Truth Table of Divide by 2	37
4.1 Synthesis Setup of Design Variables	102
5.1 Hand Analysis vs. Specification	122
5.2 Model Parameters	124
5.3 Physical Design Parameters for LO1, LO2 and LO3	125
6.1 2. 4 GHz LNA Simulation Results and Components Value	132
6.2 3. 5 GHz LNA Simulation Results and Components Value	133
6.3 2. 4 GHz MPA Simulation Results and Components value	133
6.4 3. 5 GHz MPA Simulation Results and Components value	134
6.5 Synthesis Setup of Design Variables	134
6.6 ¹ Optimized Design Variables of Power Constrained and ² Non Power Constrained	135
6.7 Broadband Amplifiers, *Non Power-Constrained	136
6.8 Properties of Control Signal Input sources	138
6.9 Calculated and Optimized Physical Design Parameters of Local Oscillators	141
6.10 Performance of Local Oscillators.	141
6.11 Optimized Design Parameters after Integration of Oscillator and Switch	145
6.12 Final Design Parameters of VSG	152
6.13 Performance Summary of VSG	152
6.14 Summary of the performance and comparison to other UWB LO Generation system	152
6.15 Simulation vs. Analysis vs. Specification	170
6.16 Real Performance vs. Specification vs. Analysis vs. Schematic Simulation	185

6.17	Summary of the performance and comparison to other I/Q Demodulator	186
A2.1	I/Q Demodulator Specifications Calculation Results	208
A2.2	Other I/Q Demodulator Specifications	208

© This item is protected by original copyright

LIST OF FIGURES

Figure		Page
2.1	Basic Architecture of a Radio Transceiver	8
2.2	A Typical Superheterodyne Receiver with a Quadrature Demodulator (Zou <i>et al.</i> , 2004; Ryyanen, 2004)	9
2.3	A Direct-Conversion Receiver (Springer <i>et al.</i> , 2002; Zou <i>et al.</i> , 2004; and Ryyanen, 2004)	11
2.4	Block Diagram of Low-IF Receiver (Pärssinen, 2001)	14
2.5	Block Diagram of the Wide-Band IF Receiver (Pärssinen, 2001)	16
2.6	A Basic Block diagram of an I/Q Demodulator	23
2.7	A Generic I/Q Demodulator for Radio Receiver	24
2.8	Basic Mixer Block Diagram	25
2.9	Diode Ring Mixer	26
2.10	Square Law Mixer	26
2.11	Triode Mixer	27
2.12	Dual-Gate MOSFET Mixer	27
2.13	Quadratic Mixer	28
2.14	Bipolar Single-Balanced Mixer	29
2.15	Double-Balanced Mixer	30
2.16	Negative g_m Circuit	31
2.17	Small Signal Equivalent Circuit	31
2.18	A Typical Tank Circuit	33
2.19	Zener Referenced Circuit	35
2.20	Block Diagram of Frequency Divider	36
2.21	A Classic Analog Frequency Divider	36
2.22	Block Diagram of Divide by 2	37
2.23	Synchronous Divide by 4 Divider	38
2.24	Asynchronous Divide by 4 Divider	38
2.25	D-Latch	39

2.26	Typical MMIC Design Flow	41
2.27	Symbol of NMOS transistor	42
2.28	Transmission Gate	43
2.29	Charge Injection when the Switch turns Off	44
2.30	Transient Response of Single NMOS Switch	45
2.31	Model of Non-Ideal Switch	46
2.32	NMOS Switch with Parasitic Capacitance	46
2.33	Shunt Feedback Amplifier	47
2.34	Shunt Feedback Amplifier with Test Current, I_{in}	48
2.35	Circuit to Define Gain	49
2.36	Circuit to Explain S_{11} - Gamma In relationship	50
2.37	Circuit to Explain S_{21}	51
3.1	Typical MMIC Design Flow	55
3.2	Proposed Design Flow	56
3.3	Basic Core Circuit	57
3.4	LNA Circuit for 2.4 GHz and 3.5 GHz	58
3.5	Single-Ended Medium Power Amplifier for RF Frequency of 2.4 GHz and 3.5 GHz.	60
3.6	Two Stage RC Feedback Amplifier	62
3.7	Mixer	63
3.8	LO-Divider Block Diagram.	67
3.9	The Block Diagram of Divide by 2 and Divide by 4	68
3.10	The Divide by 2 Circuit	68
3.11	MSDFFs (Tied Collectors) Concept	69
3.12	Clock Buffer Amplifier Circuit	70
3.13	VCO Buffer Amplifier	72
3.14	VCO Design	73
3.15	VCS Block Diagram and Current Source	74

3.16	Simplified VCS with Current Source	76
3.17	Simplified IPTAT Current Circuit	77
3.18	VCS Circuit	78
3.19	Block Diagram of Active Oscillator Solution	80
3.20	Schematic of Series-Shunt Switch	81
3.21	Cross-Coupled Oscillator with NMOS Current Source (Razavi, 2001)	83
3.22	Equivalent Circuit of Series-Shunt Switch when It is Turned On or Off.	84
3.23	Modified Series-Shunt Switch	85
3.24	Block Diagram of Variable Signal Generator	86
4.1	200 μm and 1000 μm Width Transistors	88
4.2	C_{GS} vs. Width of Transistors	89
4.3	200 μm , 400 μm , 600 μm and 1000 μm Width Transistors G_m , Drain Current vs. V_{GS} .	90
4.4	Normalized G_m , Drain Current vs. V_{GS}	91
4.5	Core Circuit	92
4.6	Parasitic Aware in the Core Circuit	93
4.7	2.4 GHz and 3.5 GHz LNA	93
4.8	2.4 GHz LNA	94
4.9	3.5 GHz LNA	95
4.10	Simulation Schematic of the PHEMT Single-Ended Medium Power Amplifier for RF Frequency of 2.4 GHz and 3.5 GHz.	96
4.11	2.4 GHz MPA Circuit	97
4.12	3.5 GHz MPA Circuit	97
4.13	Transistor Simulation Bench	98
4.14	Reverse Transmission (S_{12}) vs. Frequency ($V_{DD} = 1.5 \text{ V}$, $V_{GS} = 0 \text{ V}$, UGW = 50 μm)	99
4.15	S_{21} vs. Frequency	99
4.16	Two Stage RC Feedback Amplifier Simulation Setup	101

4.17	Goals and Optimization	102
5.1	Multiband I/Q Demodulator	105
5.2	Final Mixer	106
5.3	LO-Divider Block Diagram	109
5.4	The Block Diagram of Divide by 2 and Divide by 4	110
5.5	The Negative Resistance Circuit	111
5.6	MSDFF	113
5.7	MSDFFs (Tied Collectors)	114
5.8	Clock Buffer Amplifier Circuit	115
5.9	VCO Buffer Amplifier	116
5.10	Basic PTAT Circuit	118
5.11	Control Circuit	119
5.12	VCS Circuit	120
5.13	Emitter Follower Circuit at the Input of IC	121
5.14	Cross-Coupled Oscillator with NMOS Current Source	123
5.15	Block Diagram of Full Variable Signal Generator	126
5.16	Control Voltage Pulses	127
5.17	Biasing Circuit	127
5.18	Source Follower	129
5.19	Source Follower Frequency Response	129
6.1	Comparison Between Parasitic Aware Approach Simulation and Circuit Simulation Results	131
6.2	Mu _{load} and Mu _{source} vs. Frequency	131
6.3	Mu _{load} and Mu _{source} of the Amplifier	136
6.4	S ₂₁ vs Frequency	137
6.5	Noise Figure vs Frequency	137
6.6	Transient Response of Series-Shunt NMOS Switch with L = 1 μm	139
6.7	Transient Response of Series-Shunt NMOS Switch with L = 0.18 μm	139

6.8	Transient Response	142
6.9	Fundamental Frequency	142
6.10	Magnitude and Frequency of LO1	142
6.11	Transient Response of LO1 Connected to Switch	143
6.12	Transient Response of Output Signal from Oscillator	144
6.13	Smooth Transition of Transient Response	144
6.14	Constant Amplitude of Oscillator's Output Signal, with Modified Differential Series-Shunt Switch	145
6.15	Transient Response of First Signal Generator	146
6.16	Frequency and Amplitude of the First Signal Generated	146
6.17	Transient Response of VSG	147
6.18	Signal Generated from VSG	148
6.19	Closer Look of Signal Generated	148
6.20	Spectrum Frequency of First Frequency Generated	149
6.21	Spectrum Frequency of Second Frequency Generated	150
6.22	Spectrum Frequency of Third Frequency Generated	151
6.23	Conversion Gain vs Input Power	153
6.24	Differential Output Power vs. Input	154
6.25	Noise Figure vs. Frequency	154
6.26	LO Divider Performance at 100° C, VCC = 3.6 V	155
6.27	LO Divider Performance at – 40° C, VCC = 2.7 V	156
6.28	Phase Noise of VCO vs. Frequency	157
6.29	VCO Simulation Schematic	158
6.30	Clock Buffer Results	159
6.31	VCO Output Voltage vs. Frequency	160
6.32	Output Current of Bias Control vs. Temperature	161
6.33	Output Current of Current Sources vs. Temperature	162
6.34	Output Current of Bias Control cell vs. Time	163

6.35	Output of Current Sources vs. Time	163
6.36	Inverter Simulation Schematic	164
6.37	Inverter Output vs. Input Characteristics	165
6.38	DC Simulation Results vs. Temperature	166
6.39	DC Simulation Results vs. VCC	166
6.40	Conversion Gain (I)	167
6.41	Conversion Gain (II)	168
6.42	Conversion Gain (III)	168
6.43	Spurious Output, Conversion Gain and IIP3 at Different Frequency	169
6.44	IIP3 vs. VCC, vs. Temperature and Process Corners	169
6.45	DC Simulation Results with Parasitic Capacitance	171
6.46	Output Voltage Simulation Results with Parasitic Capacitance	172
6.47	Core Circuit Microphotograph	173
6.48	Simulation and Measurement Results of Core Circuit	173
6.49	Die Photo of the 2.4 GHz LNA	174
6.50	Die Photo of the 3.5 GHz LNA	175
6.51	S-Parameters of 2.4 GHz LNA	175
6.52	S-Parameters of 3.5 GHz LNA	176
6.53	Die Photo of the 2.4 GHz MPA	177
6.54	Die Photo of the 3.5 GHz MPA	177
6.55	S-Parameters of 2.4 GHz MPA	178
6.56	S-Parameters of 3.5 GHz MPA	179
6.57	Output Signal	180
6.58	VCO Output vs. Frequency	181
6.59	I and Q Amplitude Imbalance vs. IF Frequency	182
6.60	I and Q Phase Imbalance vs. IF Frequency	183
6.61	EVM	184

A2.1	Typical Receiver	206
A3.1	Core Circuit with Voltage Source, V_{IN}	210
A3.2	Equivalent of Transistor with Noise Sources	211
A3.3	Equivalent of Transistor with V_i	212
A3.4	Shunt Feedback Amplifier with Noisy Transistor	213
A3.5	Shunt Feedback Amplifier with Equivalent Noise Sources	213
A3.6	Shunt Feedback Amplifier with Equivalent Noise Sources and Termination for Noise Figure Calculation	214
A4.1	A Unit Square Wave	215
A4.2	Ideal Mixer Output Spectrum	216
A5.1	Degenerated Differential Amplifier	218
A5.2	Differential-Mode Equivalent Half Circuit	220
A5.3	Small-Signal Equivalent Circuit of the Differential-Mode Equivalent Half Circuit	221
A5.4	Noise Representation of a Transistor at High Frequency	222
A5.5	Conventional Noise Representation	223
A5.6	Noise Factor Representation	224
A5.7	Basic Block Diagram of a Feedback System	225
A6.1	Mixer Layout	229
A6.2	Negative Resistance Circuit Layout	230
A6.3	MSDFF Layout	231
A6.4	MSDFFs (tied collectors) Layout	232
A6.5	Clock Buffer Amplifier Layout	233
A6.6	VCO Buffer Amplifier Layout	234
A6.7	VCSL Layout	235
A6.8	VCSH Layout	236
A6.9	Control Circuit Layout	237
A6.10	Standard Bondpad	238

© This item is protected by original copyright

LIST OF SYMBOLS

Ω	Ohm
γ	Noise parameter, $\gamma = 2/3$ for long-channel
δ	Coefficient of gate noise, $\delta = 2\gamma = 4/3$ for long-channel
α	Noise parameter, $\alpha = g_m / g_{d0}$
Γ	Reflection coefficient
Γ_S	Reflection coefficient looking into the source
Γ_{in}	Reflection coefficient looking into the input
Γ_L	Reflection coefficient looking into the load
Γ_{out}	Reflection coefficient looking into the output
μ_n	Mobility of electron
μ_p	Mobility of hole
ξ	Noise parameter of the uncorrelated portion of the transistor's gate noise
ξ_1	V_{DS} to V_{OV} ratio
κ	Noise parameter of the correlated portion of the transistor's gate noise
χ	Noise parameter that includes both correlated and uncorrelated portions of the transistor's gate noise
ρ	$\rho = V_{OV} / LE_{sat}$
ϵ_0	Permittivity of free space, $\epsilon_0 = 8.854 \times 10^{-12}$ F/m
λ	Wavelength of the frequency of operation
A_d	Area drawn
A_v	Voltage gain
A_{vo}	Open-circuit voltage gain
B_c	Correlation susceptance
B_{opt}	Optimum susceptance
B_S	Source noise susceptance

B_{system}	System bandwidth
c	Correlation coefficient, $c = j0.395$ for long-channel devices
C_a	Areal capacitance
C_c	Coupling capacitor
C_{db}	Drain-Body capacitance
C_f	Feedback capacitor
C_{gd}	Gate-Drain capacitance
C_{gs}	Gate-Source capacitance
C_{gsn}	Gate-Source capacitance of NMOS
C_{gsp}	Gate-Source capacitance of PMOS
C_{gsT}	Total Gate-Source capacitance
C_{light}	Speed of light, $C_{\text{light}} = 3 \times 10^8$ m/s
C_{ox}	Oxide capacitance of NMOS
C_{oxn}	Oxide capacitance of PMOS
C_{oxp}	Oxide capacitance
C_p	Capacitance per unit periphery
C_t	Total capacitance
d	Largest dimension of the design
E_b	Average bit energy
$(E_b/N_t)_{\text{eff}}$	Average bit energy to noise and interference power spectral density minimum ratio
E_C	Average energy per PN chip
\bar{e}_n	External voltage noise generator
E_{sat}	Field strength at which the carrier velocity has dropped to one half the value extrapolated at low-field mobility
f	Frequency
F	Noise factor
f_{block}	Frequency of the block signal

f_{cw}	Spurious response frequencies
f_{IF}	Frequency of the IF Signal
f_{LO}	Frequency of the LO Signal
F_{min}	Minimum noise factor
F_{min}^o	Minimum noise factor for the classical noise matching input stage of the LNA
f_{RF}	Frequency of the RF signal
f_T	Transition frequency
F_{UW}	Frequency of unwanted signal
F_{UW1} (CW)	Frequency of the first unwanted signal of the CW nature
F_{UW2} (Modulated)	Frequency of the second unwanted signal of the modulated nature
f_{wanted}	Frequency of the wanted signal
G_c	Correlation conductance
g_{d0}	Drain-Source conductance at 0 V_{DS}
G_f	Conductance of C_f
g_g	Real, noiseless conductance in the gate circuit
g_m	Transconductance of the transistor
G_m	Transconductance of the circuit
g_{mb}	Body-effect transconductance of the MOSFET
G_{m-C}	Transconductance-Capacitor
G_{m_eff}	Effective transconductance of the circuit
g_{mT}	Total transconductance
G_n	Conductance contributing to thermal noise due to $\overline{i_n^2}$
G_{opt}	Optimum conductance
G_S	Conductance contributing to thermal noise due to $\overline{i_s^2}$ or source conductance
$I_{blocking}$ (CW)	Blocking signal (CW) band power spectral density

I_c	Noise current correlated with e_n
I_D	DC drain current
$\overline{i_d^2}$	Channel thermal noise source
i_g^2	Shunt noise current to g_g
$\overline{i_{g,c}^2}$	Gate noise current source correlated with the drain noise
$\overline{i_{g,u}^2}$	Gate noise current source uncorrelated with the drain noise
$\overline{i_n}$	External current noise generator
I_{or}	The total transmit power spectral density of the forward link at the base station antenna connector.
\hat{I}_{or}	The received power spectral density of the forward link as measured at the UE antenna connector.
I_{ouw}	Unwanted signal specified by the W-CDMA standard for linearity tests
i_s	Noise source
i_u	Noise current uncorrelated with e_n
k	Boltzmann constant, $k = 1.38 \times 10^{-23} \text{ J/}^\circ\text{K}$
K	Stability factor
K_{ox}	Relative permittivity of silicon dioxide
$k \Omega$	kilo-ohm
L	MOSFET's channel length
L_d	Length drawn
L_g	Gate inductor
L_s	Source inductor
N_o	Noise spectral density
N_t	Noise and interference power spectral density
$P_{2\text{ndorder(blocker)}}$	Power of the second-order products of the blocker signal
P_{allowed}	Noise power allowed
P_{AVN}	Power available from the network

P_{AVS}	Power available from the source
P_{BLeak}	Power of the blocker leakage
$P_{BLOCKER (in-band)}$	Power of the in-band blocker
$P_{CW(interferer)}$	Power of the CW interferer signal
P_D	Power dissipated by the LNA
P_d	Perimeter
$P_{DPCH(RX)}$	Power of the dedicated physical channel at the receiver
$P_i(\text{acceptable})$	Maximum allowable interference level
P_{INT}	Power of the interfering signal
$P_{intermodulation}$	Power of an intermodulation signal
$P_{modulated(interferer)}$	Power of the modulated interferer signal
P_N	Noise power
P_{N+I}	Power of noise + interference
$P_{N(actual)}$	Actual noise power
$P_{N(max)}$	Maximum allowable noise power
$P_{N(osc)}$	Noise power of the oscillator
P_o	A constant which is dependent on the process parameters v_{sat} and E_{sat}
P_{TxLeak}	Power of the Tx leakage signal
q	Electronic charge, $q = 1.6 \times 10^{-19}$ C
Q_{in}	Quality factor of the input stage
Q_{in,opt,P_D}	Optimum quality factor of the input stage
Q_{ind}	Quality factor of the inductor
Q_{opt}	Optimum quality factor
$Q_{parallel}$	Quality factor of the parallel output impedance
Q_S	Quality factor in the form of the actual source (input) conductance
Q_{series}	Quality factor of the series output impedance