OPTIMIZATION OF P-I-N RECTIFIER DIODE FOR YIELD AND ROBUSTNESS IMPROVEMENT USING DOE

By

CHEH CHAI MEE
(1431711484)

A thesis submitted in fulfillment of the requirements for the degree of
Master of Science in Nanoelectronic Engineering

INSTITUTE OF NANO ELECTRONIC ENGINEERING
UNIVERSITI MALAYSIA PERLIS

2016

ACKNOWLEDGEMENT

I would like to thank University Malaysia Perlis (UniMAP), School of Microelectronic Engineering (SoME) and specifically Institute of Nano electronic Engineering (INEE) for providing me with exceptional 2 years of trials and tribulations. Most of all, the excellent facilities are truly appreciated.

I wish to express my greatest gratitude to project supervisor, Ir. Dr. Mohd Khairuddin Md Arshad for his encouragement and advices for my academic and research efforts. I have learned a lot from Dr. Mohd Khairuddin, his expertise in fabrication and device theory have made me gain a lot of knowledge in device knowledge.

Last but not least, a very big thank you to my beloved family for their constant encouragement and support in my research studies these two years. I would not have gotten so far without their support.

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LIST OF ABBREVIATIONS

IR	Reverse leakage current
VR	Reverse Voltage
VF	Forward Voltage
DVR	Delta Reverse Voltage
TRR	Reverse recovery time / Lifetime
DOE	Design of Experiment
UIS	Unclamp Inductive Surge
SRP	Spread Resistance Profiling
HMDS	Hexamethydisilane
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OFAT	One factor at a time
ns	nano second

LIST OF SYMBOLS

IR	Reverse leakage current
VR	Reverse Voltage
VF	Forward voltage
TRR	Reverse recovery time / Lifetime
VPT	Punch Through Voltage
Ec	Electric Field
E_1	Electric Field for punch through
W_p	Thickness of the intrinsic region
q	Charge
N_{AP}	Donor concentration for punch through
$^{\varepsilon}S$	Dielectric constant for Silicon
n_i	Intrinsic resistivity
τ_{SC}	Space charge generation of lifetime
J_{SC}	Space charge generation leakage current
J_{DP}	Diffusion current from the P or P+ region.
J_{DN}	Diffusion current from the N or N+ region.
D_p	Holes diffusion constant
D_n	Electron diffusion constant
V_a	Potential difference
N_p	Donor concentration
L_p	Diffusion length of the N side junction
Si	Silicon
O_2	Oxygen molecule

SiO_2	Silicon Dioxide
$2H_2O$	Water molecule
$2H_2$	Hydrogn moleclue
ΔT	Amount of material remove in etching
T	Time
n(x)	Carrier concentration in SRP
p	Sample resistivity in SRP
μ	mobility in SRP
Δz	Depth Profing in SRP
A	Bevel Angle in SRP
X	Probe movement of bevel distance
H	High matrix in DOE
C	Center matrix in DOE
L	Low matrix in DOE
Ωcm	resistivity in ohm
μm	micron meter

PENGOPTIMUMAN DIOD PENERUS KUASA P-i-N UNTUK PENAMBAHBAIKAN PEROLEHAN DAN KEBOLEHTAHANAN DENGAN MENGGUNAKAN KAEDAH REKABENTUK UJIKAJI.

ABSTRAK

Penerus kuasa (penerus P-i-N) merupakan salah satu diod yang digunakan secara meluas dalam peranti semikonduktor berkuasa tinggi untuk perlindungan litar. Penggunaan meluas ini disebabkan oleh kecemerlangannya untuk menyekat voltan balikan dan masa pensuisan yang pantas. Hasilnya, kajian terhadap penerus kuasa tersebut untuk membuatkannya suatu peranti yang lebih mantap dan berdaya saing dalam pasaran menjadi tidak terbatas, bertujuan untuk penambahbaikan yang berterusan ke atas ciri-ciri elektrikalnya. Secara umum, penerus P-i-N adalah terdiri daripada simpang PN yang terdop tinggi dengan kawasan hakiki terdop rendah diapit di antaranya. Ciri-ciri tersebut telah membolehkan reka bentuk setinggi 1000 V voltan balikan diod dengan masa pensuisan yang rendah. Tesis ini menerangkan kerja-kerja penyelidikan yang telah dilakukan terhadap penerus kuasa dengan meneroka ciri-ciri peranti dan mengoptimumkan sambutan masuk menggunakan rekabentuk eksperimen (*Design of Experimen, DOE*) berdasarkan parameter seperti spesifikasi lapisan epitaxi, masa resapan simpang dan juga proses-proses fabrikasi dalaman lain, untuk menghasilkan peranti yang dikehendaki dan untuk meningkatkan perolehan. Ciri-ciri elektrikal utama iaitu masahayat pulih balikan (*reverse recovery lifetime*), voltan balikan (*reverse voltage*) dan arus balikan (*leakage current*) telah dikaji dan dianalisis. Keputusan menunjukkan bahawa dengan pelaksanaan ketebalan serta kerintangan epitaxi yang dioptimumkan, membolehkan penerus kuasa P-i-N diod berupaya menahan voltan balikan yang tinggi. Ketebalan epitaxi optimum untuk peranti berkeupayaan 600 V adalah pada 96 µm. Ketebalan lapisan epitaxi merupakan faktor dominan berbanding dengan kerintangan epitaxi dan masa resepan boron. Seterusnya perubahan dalam masa resapan simpang (*drive in time*) menunjukkan bahawa, ia memberi hubungan langsung antara kedalaman simpang (*junction depth*) P-i-N dengan voltan balikan (*reverse voltage*) untuk peranti berkeupayaan 200 V. Setiap penambahan selama 60 minit masa resapan simpang akan meningkatkan voltan balikan sebanyak 30 V. Akhir sekali, siasatan tentang masahayat pulih balikan dan voltan hadapan (*forward voltage*) dalam penerus kuasa diod telah dilaksanakan. Faktor-faktor yang dikaji adalah masa resapan dan suhu resapan platinum. Keputusan yang diperolehi menunjukkan bahawa suhu tinggi serta masa resapan platinum yang pendek akan menghasilkan penerus kuasa diod berkeupayaan 600 V yang sesuai serta memenuhi spesifikasi voltan hadapan iaitu 1.8 V serta masahayat pulih balikan iaitu 27 ns. Semua data yang diperolehi daripada pengujian elektrikal telah menunjukkan bahawa, diod yang dihasilkan adalah berfungsi dengan baik, dengan hasil pengolehan yang lebih baik apabila parameter yang kritikal seperti masahayat pulih, voltan balikan dan voltan hadapan terhasil seperti yang dikehendaki.

OPTIMIZATION ON P-i-N POWER RECTIFIER DIODE FOR YIELD AND ROBUSTNESS IMPROVEMENT USING DOE

ABSTRACT

The Power Rectifier (P-i-N rectifier) is one of the widely used diode in high power semiconductor devices as circuit protection. This popularity comes from excellent reverse voltage blocking and fast switching time. As a result, the exploration on the power rectifiers to make the device more robust and competitive in the market is boundless, which aims for continuous improvement on the electrical characteristics. In general, the P-i-N rectifier is consists of a highly-doped P-N junction with a low doped intrinsic region sandwiched in between the regions. Such characteristics have made the design of as high as 1000 V reverse voltage diode is possible by lowering the switching time. This thesis describes the research work done on the power rectifier by exploring the device characteristics and optimizing the input responses using Design of Experiment (DOE) techinique. Parameter such as epitaxial layer specification, junction drive time and also other internal fabrication processes were optimized, to produce a desired device robustness and yield improvement. The main electrical characteristics namely reverse recovery lifetime, reverse voltage, reverse leakage current and such, were investigated and analyzed. The results show that with implementation of optimized epitaxial thickness and resistivity, the P-i-N power diodes were able to withstand high reverse voltage. The optimum epitaxial thickness for 600 V device is at 96 µm. The epitaxial thickness is a dominant factor as compared to epitaxial resistivity and boron diffusion time. Next, the variation in junction drive time shows a direct relationship between the junction depth of the P-i-N rectifier to the reverse voltage for 200 V device. Each additional 60 minutes in boron diffusion time will increase the device reverse voltage by 30 V. Lastly, the investigations are about reverse recovery lifetime and forward voltage of the power diode. The factors to be investigated are platinum diffusion time and diffusion temperature. From the result, it show that high temperature and low platinum diffusion time produces an optimum 600 V power rectifier that fit forward voltage specification at 1.8 V and reverse recovery lifetime of 27 ns. This shows the forward voltage of the power rectifier is inversely proportional to the reverse recovery lifetime. All the data collected from the electrical test have demonstrates the fabricated diodes are functional with better yield and robustness when the critical parameters such as reverse recovery lifetime, reverse voltage and forward voltage meet the pre-determined requirement.

CHAPTER 1

INTRODUCTION

1.1 Background of research

A material that has an ability to conduct electric current in between conductors and insulators is known as semiconductor (Floyd, 2008). In semiconductor technologies, a diode is formed when a piece of intrinsic silicon is doped with n-type dopant and another part is doped with p-type dopant. A p-n junction will be formed at the boundary between these two regions (Baliga, 1996). An evolution of p-n diode happened when there is an extra intrinsic layer formed between p-type and n-type dopants. The P-i-N rectifier is one of the very first semiconductor device developed for power circuit applications (Baliga, 1996). Figure 1.1 illustrates the p-i-n diode structure.

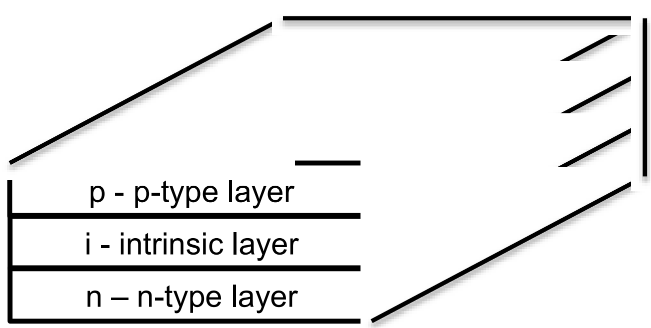

Figure 1.1: 2D structural layer P-i-N diode

P represents the p-type layer, n represents the n-type layer, i represents the intrinsic layer that stack in between p-type and n-type layer. The intrinsic layer makes this diode ideal for fast switches. Another unique characteristic for P-i-N rectifier is its low voltage drop and high breakdown voltage. The width of the low-doped base region, define the reverse breakdown of the P-i-N rectifier. Basically, P-i-N rectifier widely used in power electronic applications as their central layer can withstand high voltages. There are quite a number of studies for the past decades to explain the behavior of small-signal low power p-n junction diodes (Gandhi, 1977; Hall, 1952; Jayant Baliga, 1992; Jubadi & Noor, 2010; Kingston, 1954; Mazhari, Sinha, & Dixit, 2006; Moll, 1964; Pendharkar, Trivedi, & Shenai, 1996; Salah et al., 2007; Sze, 1995; Tsukuda, Sakiyama, Ninomiya, & Yamaguchi, 2009) and high-power P-i-N rectifier (Abiri, Salehi, Kohan, & Mirzazadeh, 2010; Cai, Zhang, Ren, & Sheng, 2013; Cappelluti et al., 2006; Gaur et al., 2015; Jablonski, 1998; Jubadi & Noor, 2010; Polyakov et al., 2000; Salah et al., 2007; Sawant & Baliga, 1999; Shuhaimi et al., 2010; Xue, Fu, & Zhang, 2016)

1.2 Problem statements

This research is greatly motivated by the great interest in understanding the functions of power rectifier. In general, power rectifiers are widely used in power industry. Its function includes protecting the circuit by blocking a huge amount of reverse voltage flow through the circuit. Besides circuit protection, power rectifier also has one interesting feature which is fast switching function. The fast switching enables the rectifier to turn from on-state to off state faster.

Two commercially available power rectifier devices are the interest in this work, i.e. 200V and 600V. The low yield for these two types of diode encourages us to explore and to understand the problem. In this thesis, we propose to solve the 600V power rectifiers through epitaxial optimization and also through platinum DOE approach. Two different approaches are applied to solve the multiple low yield issue such as low reverse voltage and high forward voltage. This is to explore a good working window for a 600V power rectifier. In device theory, the reverse voltage of a power rectifier is controlled by the epitaxial layer of a substrate. Besides epitaxial layer, the junction formed through device fabrication is also a key factor to control and to design a power rectifier. For 600V power rectifier research approach, the key analysis and investigation of exploring a good working window is assisted by Design of Experiment (DOE) method.

As for 200 V power rectifiers, the research is focus in the junction depth of the I-region to the reverse voltage of a power rectifier. As discussed in previous paragraph, the reverse voltage of the power rectifier is governed by the window of the epitaxial layer and also as well as the junction depth form through device fabrication. There is certain amount of diffusion duration to form the junction of a power rectifier and the certain junction depth will yield a certain amount of reverse voltage. In this 200 V available commercial device, the relation of drive time will be studied and explored. By understanding the relation of drive time to reverse voltage, different voltage rating rectifiers in market could be produced depending on the customer's application. The reason epitaxial approach is not applying in this research is because 200 V device have a lower epitaxial thickness compare to 600 V device. Hence, the junction depth approach is more appropriate.

1.3 Research objectives

The objectives of the research can be summarized as follows.

- To improve 600 V power rectifier robustness through epitaxial optimization using DOE approach.
- To evaluate and explore the junction depth (validation analysis through spread resistance profiling) of an intrinsic region to 200 V device reverse voltage.
- To find a trade off curve between the forward voltage drop and reverse recovery lifetime of a 600 V power rectifier.

A commercially available 600 V P-i-N rectifier was used to investigate the effects of changes in i-region width on the current-voltage (I-V) performances. Basically, the main yield loss of this device is related to low reverse breakdown and high reverse leakage. Low yield is not only related to reduce of profit margin, but also caused the diode not robust for power device. Since p-i-n rectifier operates in a thickness-limited mode, which is controlled by the width of an i-region, the factors need to be taken into consideration is the epitaxial specification which includes epitaxial thickness and epitaxial resistivity. The given specification for epitaxial thickness is from 89 - 102.7μm with resistivity ranges from 30 – 42 Ωcm. High epitaxial thickness which will lead to high reverse voltage (VR) and high forward voltage (VF) since VR is proportional to VF.

This P-i-N rectifier has a relatively small operating margin for forward and reverse breakdown voltage. Despite that, there are a few factors that should be taken into consideration for improving the device yield and performance, which should reflect to robustness of production variation.

The attention will focus on the depth of the intrinsic region and how it impacts the reverse voltage of the 200 V power devices. In this thesis, a commercially available 200

V P-i-N rectifier was used to investigate the variable depth in I-region on the current-voltage (I-V) performances. Initially, the depth of the I-region is a constant and it will only be changed during diode wafer fabrication. This is due to N+ is the bulk substrate and intrinsic region is the epitaxial layer. Both of the epi and substrate have a constant depth. A diode is formed when the P+ dopant is diffused into the intrinsic region during wafer fabrication. The diffusion of the P+ dopant into intrinsic region will cause the junction depth of the I-Region to be shallowed. Diode formation is formed by diffusing a P+ dopant into intrinsic region. The P-i-N rectifier structure is illustrated in Figure 1.2, where the junction depth variation (D) is controlled by the depth of P+ impurities dopant formed during fabrication.

Since P-i-N rectifier operates in a thickness-limited mode, which is, controlled by the depth of an I-region, different depth in P-region during thermal diffusion will lead to different junction depth in I-region. The deeper the junction depth of the P-region, the shallower will be junction depth of the I-region. This is because more of the intrinsic region is consumed to form a P-region. Thus in this work, we tune the depth of the P-region to study the effect of reverse voltage and I-region depth as illustrated in Figure 1.2.

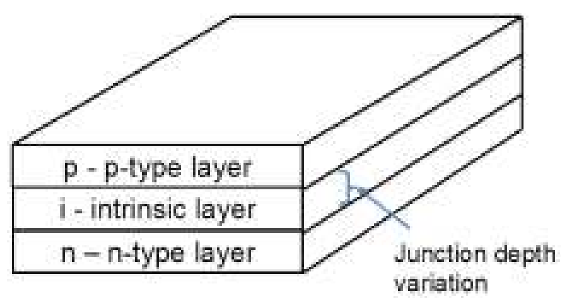

Figure 1.2: 2D structural layer P-i-N diode with junction depth variable

The last objective in this thesis is to find a trade-off graph between forward voltage (VF) and reverse recovery time (TRR) for a 600 V power rectifier. The reverse recovery time of a diode is one the key parameter in power electronics market. TRR is also referred as the time taken for the diode to switch from forward bias to reverse bias. The reverse recovery time is the combination of the storage time and recovery time. During forward bias, there is a buildup of minority carriers at the edge of the depletion region. The minority carriers will diffuse to the opposite material during reverse bias and causing the storage time. Once the minority carriers migrate they will diffuse and recombine where it is known as the recovery time. To produce a diode with fast switching speed, diodes are often doped with impurities such as gold and platinum to improve its lifetime. This work presents the lifetime improvement of a power rectifier through platinum diffusion in the intrinsic region in between P-N junction.

1.4 Research scopes

The work scope in this research is mainly divided into three main parts. The initial stage of this research includes identifying the existing problem of both low and high voltage power rectifiers. Second stage of the work scope is about looking for the improvement of power rectifier via DOE approach after the problems have been identified. In the second stage, fabrication of power rectifier is executed to get the real result. In the third part, the electrical testing and also device characterization are performed using spread resistance profiling (SRP) analysis and also the JMP software. The core of the electrical testing is to validate the hypothesis in earlier stage.

The work scope in this research begins with problem identification. In this part, the electrical properties of the power rectifiers are studied. The DOE method is applied in the second part together with power rectifier fabrication to process samples for analysis and verification. Fabrication of a power rectifiers included oxidation, photolithography, etching and metallization process.

Once fabrication completed, the samples are tested for its functionality. The purpose of this third part is to verify the hypothesis that made earlier. The functionality test included electrical testing to check for the forward voltage, reverse leakage current and also the reverse voltage of a power rectifier.

Besides non- destructive analysis, we also performed destructive analysis to validate the hypothesis. The destructive analysis in this work scope includes Spread resistance profiling (SRP). SRP is a technique used to check for the junction depth together with the resistivity of a rectifier along the analysis.

1.5 Thesis Overview

In general, this thesis consists of five Chapters. First chapter provides an overview of this research to the readers. This also includes the objectives and the importance of the research.

The literature review of power rectifier and evolution of power rectifier are discussed in Chapter 2. This chapter will present to the audience the theory of the power rectifiers, the rectifiers function and application in semiconductor market.

After an account of the literature review of the power rectifier in Chapter 2, the fabrication process of the power rectifier are described in the following chapter. Besides fabrication process, the overview of Design of Experiment (DOE) and Spread Resistance Profiling (SRP) are also elaborated on this chapter. Chapter 3 presents the methodology that we used to verify the hypothesis that made in Chapter 1.