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**Simulation of Graphene Band Structure
and Fabrication of Graphene Field Effect Transistor**

by

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2018

A thesis submitted in fulfillment of the requirements of the degree of
Master of Science (Microelectronic Engineering)

**School of Microelectronic Engineering
UNIVERSITI MALAYSIA PERLIS**

2018

ACKNOWLEDGEMENT

Alhamdulillah this thesis has finally come to an end.

First of all I would like to thank my supervisor Dr Nor Syarifah Faezah bt Sabki for her guidance and support through out my study in UNIMAP. Thank you Dr for being such an understanding and supportive supervisor. All your guidance and advice had been a wonderful help for me in completing this thesis. I would also want to thank all the technicians in FA lab and Nano lab for the help and support that had been given. Thank you all!

To my husband Dr Ahmad Kadri b Junoh who has been my biggest supporter for my study, thank you for this journey started because of you. To my children Ahmad Afiq, Siti Amni and Ahmad Adib, I would like to dedicate this work to all of you. May this work become the inspiration to all of you. To my siblings Fauzan, Samsul, Tinie, Effa, Tom, Ikah and Adik Ilah, thank you for supporting Kak Ina. Last but not the least I would like to thank my mother Pn. Hasnah bt Mustapha and my mother in law Pn Rahimah bt Samat for the support and advice. Thank you Ma.

TABLE OF CONTENTS

| | PAGE |
|---|-------------|
| DECLARATION OF THESIS | ii |
| ACKNOWLEDGEMENT | iii |
| TABLE OF CONTENTS | iv |
| LIST OF TABLES | vi |
| LIST OF FIGURE | vii |
| LIST OF ABBREVIATION | xi |
| LIST OF SYMBOLS | xii |
| ABSTRAK | xiii |
| ABSTRACT | xiv |
| CHAPTER 1 INTRODUCTION | 1 |
| 1.1 Overview of Graphene | 1 |
| 1.2 Problem Statement | 2 |
| 1.3 Research Objectives | 5 |
| 1.4 Research Scope. | 6 |
| 1.5 Thesis Outline | 7 |
| CHAPTER 2 LITERATURE REVIEW | 9 |
| 2.1 Introduction | 9 |
| 2.2 Graphene | 9 |
| 2.2.1 Physical Properties of Graphene and Energy Dispersion | 10 |

| | | |
|---|---|-----------|
| 2.3 | Band Gap in Graphene | 14 |
| 2.3.1 | Graphene Preparation | 17 |
| 2.4 | Graphene Transfer Process | 19 |
| 2.5 | Graphene Field Effect Transistor | 20 |
| 2.5.1 | Transfer Characteristics of GFET | 22 |
| 2.5.2 | Charge Carrier Mobility | 23 |
| 2.5.3 | Charge Carrier Concentration | 25 |
| 2.6 | Summary | 26 |
| CHAPTER 3 METHODOLOGY | | 28 |
| 3.1 | Introduction | 28 |
| 3.2 | Simulation of graphene band structure | 28 |
| 3.2.1 | Monolayer, Symmetrical Bilayer and Asymmetrical Bilayer Graphene. | 29 |
| 3.2.2 | Graphene doped with hetero atoms | 31 |
| 3.3 | Fabrication of Graphene Field Effect Transistor (GFET) | 33 |
| 3.3.1 | Graphene Transfer Process | 34 |
| 3.3.2 | The Transfer Process of Graphene to SiO ₂ /Si Surface. | 40 |
| 3.3.3 | The fabrication of GFET. | 42 |
| 3.3.4 | Characterization | 52 |
| 3.4 | Summary | 56 |
| CHAPTER 4 RESULTS AND DISCUSSION | | 57 |
| 4.1 | Introduction | 57 |
| 4.2.1 | Monolayer, Symmetrical Bilayer, Asymmetrical Bilayer Graphene. | 58 |
| 4.2.2 | Graphene doped with hetero atoms | 60 |
| 4.3 | Optimization of Graphene Transfer Process for GFET Fabrication | 69 |

| | | |
|---|---|------------|
| 4.3.2 | Graphene Field Effect Transistor (GFET) | 76 |
| 4.3.3 | Characterization of GFET | 77 |
| 4.4 | Summary | 87 |
| CHAPTER 5 CONCLUSION & FUTURE WORK | | 89 |
| 5.1 | Conclusion. | 89 |
| 5.2 | Future work | 91 |
| REFERENCES | | 92 |
| APPENDIX A LIST OF PUBLICATION | | 102 |

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LIST OF TABLES

| | PAGE | |
|------------|---|----|
| Table 3.1 | Monolayer graphene structures doped with different concentration of boron and oxygen atoms. The position of boron and Oxygen are differentiated based on label 1 & 2. | 33 |
| Table 4.1 | A summary of energy band gap for monolayer, symmetrical and asymmetrical bilayer graphene | 60 |
| Table 4. 2 | Energy band gap for graphene doped with B atom | 64 |
| Table 4. 3 | Energy band gap for graphene doped with O atoms. | 67 |
| Table 4. 4 | Electron and Hole Mobility for GFETs in Sample 1 | 84 |
| Table 4. 5 | Electron and Hole Mobility for GFETs in Sample 2 | 86 |

LIST OF FIGURE

| | | PAGE |
|-------------|---|-------------|
| Figure 2. 1 | Hexagonal pattern of graphene | 10 |
| Figure 2.2 | The energy dispersion variations of graphene lattice (Davood Fathi, 2011) | 14 |
| Figure 2.3 | Isolation of graphene through exfoliation of graphite. | 17 |
| Figure 2.4 | Chemical Vapor Deposition (CVD) for Graphene Growth on Nickel (Al Shurman &Naseem , 2014.) | 18 |
| Figure 2.5 | Typical transfer characteristics for two MOSFETs with large-area graphene channels.(Shwietz, 2010) | 22 |
| Figure 2.6 | Graphene Field Effect Transistor (GFET) configuration with (a) back gate (b) top gate | 21 |
| Figure 2.7 | Transfer characteristic of GFET for I_{DS} vs V_{DS} (Shweirz , 2010) | 23 |
| Figure 3.1 | Side view of (a) monolayer graphene (b) symmetrical bi-layer graphene and (c) asymmetrical bi-layer graphene | 31 |
| Figure 3.3 | Complete process of PMMA solution preparation | 38 |
| Figure 3.4 | A complete process of PDMS solution preparation. | 39 |
| Figure 3.5 | The graphene Transfer Process by Using Polymeric Layer Method. | 41 |
| Figure 3. 6 | The GFET structure fabricated in this work with gate length, L, source and drain width, W, gate width, WTG, gate oxide thickness, TGox, and buried oxide thickness, TFox. | 42 |
| Figure 3. 7 | Mask for gate oxide. | 44 |

| | | |
|-------------|--|----|
| Figure 3.9 | Oxidation Furnace | 46 |
| Figure 3.10 | Metal evaporation's process. | 48 |
| Figure 3.11 | The gate oxide pattern transfer and oxide etch | 49 |
| Figure 3.12 | Al pattern transfer and Al etch | 51 |
| Figure 3.13 | Voltage bias for current- voltage transfer characteristic | 54 |
| Figure 3.14 | Voltage bias for output transfer characteristic | 55 |
| Figure 3.15 | Graph of conductivity versus charge carrier concentration | 56 |
| Figure 4.1 | Band structures for (a) Monolayer graphene (b) Symmetrical bilayer graphene | 58 |
| Figure 4.2 | Band structure for asymmetrical bilayer graphene. | 59 |
| Figure 4.3 | Band structures of graphene doped with B in the same sub lattice (B1). The B concentrations are at (a) 3 %, (b) 6% and (c) 9%. | 61 |
| Figure 4.4 | Band structures of graphene doped with B in different sub lattice 1 (B2). | 62 |
| Figure 4.5 | Band structures of graphene doped with B in different sub lattice 2 (B3). | 63 |
| Figure 4.6 | Band structures for graphene doped with oxygen in same sub lattice (a). 3 % Oxygen doped. (b). 6%O. (c).9% O. | 65 |
| Figure 4.7 | Band structures for graphene doped with O in different sub lattice 1 (a). 6 % O. (b). 9%O. | 66 |
| Figure 4.8: | Band structures for graphene doped with O in different sub lattice 2 (a). 6 % O. (b). 9% O. | 67 |
| Figure 4.9 | The energy band gaps for graphene doped with B and O at different concentration, and different position in graphene sub- | |

| | | |
|---------------|---|----|
| | lattices. Refer Table 3.1 in Chapter 3 for the position of the atoms in graphene sub lattices. | 68 |
| Figure 4.10 | AFM images of (a) graphene on Cu and (b) graphene layer transferred to SiO ₂ /Si surface. | 70 |
| Figure 4. 11 | Optimization of the graphene coverage by applying pressure to the top of PDMS. The approaches are by (a) pressing the PDMS several times with finger tip in 10s (Sample 1), (b) pressing the PDMS constantly with finger tips in 10s (Sample 2) and (c) pressing the PDMS constantly using a wooden block (Sample 3). | 71 |
| Figure 4. 12 | Transferred graphene observed under optical microscope (a) Sample 1: major coverage of broken graphene layer (b) Sample 2: better coverage of graphene layer with broken graphene around the edges (c) Sample 3: graphene layer with good coverage | 72 |
| Figure 4.13 | HPM images of transferred graphene layer on SiO ₂ /Si (a) untreated graphene (b) graphene has undergone several cleaning process after the transfer. | 73 |
| Figure 4. 14 | I-V curves of transferred graphene layer obtained from Sample 3 after cleaning process by immersion in acetone in three immersion stages represented by first immersion as C1, second immersion as C2 and third immersion as C3. | 75 |
| Figure 4.15 | Two different samples of fabricated GFETs. (a) Sample 1(T_{Gox} of 63 nm) and (b) Sample 2(T_{Gox} of 83 nm) | 77 |
| Figure 4. 16 | Current -Voltage (Drain to source current, I_{ds} vs Top Gate Voltage, V_{tg}) Transfer Characteristic for GFETs in Sample 1. | 79 |
| Figure 4. 17 | Current- Voltage Transfer Characteristic for GFETs in Sample 2 | 80 |
| Figure 4. 18: | Output Characteristic (I_{ds} versus V_{ds}) for GFETs in Sample 1. | 81 |

| | | |
|--------------|---|----|
| Figure 4. 19 | Output Characteristic (I_{ds} versus V_{ds}) for GFETs in Sample 2. | 82 |
| Figure 4. 20 | The relation between carrier mobility and channel length for Sample 1 | 84 |
| Figure 4. 21 | The relation between mobility with channel length for Sample 2. | 85 |
| Figure 4. 22 | Comparison of electron mobility in Sample 1 and Sample 2 | 87 |

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LIST OF ABBREVIATION

| | |
|-------------------|----------------------------------|
| AFM | Atomic-Force Microscopy |
| Al | Aluminum |
| aq | aqueous |
| B _{ox} | Buried Oxide |
| Cu | Copper |
| CV | Current-Voltage |
| CVD | Chemical vapor deposition |
| DFT | Density Functional Theories |
| DI | De ionized |
| FeCl ₃ | Iron Chloride |
| GFET | Graphene Field Effect Transistor |
| HPM | High Power Microscope |
| PDMS | Polydimethylsiloxane |
| PMMA | Poly (methyl methacrylate) |
| SE | Semi empirical |
| SiO ₂ | Silicon Dioxide |
| T _{Box} | Thickness of buried oxide |
| T _{FOX} | Thickness of field oxide |
| TKMG | Transistor Kesan Medan Graphene |
| 2D | Two dimensional |

LIST OF SYMBOLS

| | |
|----------------------------|----------------------------|
| cm^2V^{-1} | Centimetre square per volt |
| e | Elementary charge |
| eV | Electron volt |
| μA | Micron Ampere |
| μ_e | Electron mobility |
| μ_h | Hole mobility |
| μm | Micron meter |
| I_{ds} | Drain to source current |
| n | Charge concentration |
| n_e | Electron concentration |
| n_h | Hole concentration |
| Sm^{-1} | Siemens per meter |
| V | Volt |
| V_{DS} | Drain to source voltage |
| V_{tg} | Top gate voltage |
| σ | Conductivity |

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Simulasi Struktur Gelombang Graphene dan Fabrikasi Transistor Kesan Medan Graphene

ABSTRAK

Tesis ini membentangkan satu pendekatan dalam mengkaji graphene untuk elektronik digit, dan juga analog. Untuk aplikasi elektronik digit, kerja ini memfokuskan kepada pembukaan dan perubahan jurang jalur graphene satu lapisan berdasarkan kepada kemasukan atom-atom dopan, dengan menggunakan pensimulasi AtomixKit daripada Quantum Wise. Dua set simulasi telah dijalankan, yang mana, untuk mengkaji struktur jalur graphene berdasarkan kepada kesan lapisan graphene yang asimetrik dan mendop graphene satu lapisan dengan atom-atom boron dan oksigen. Keputusan telah menunjukkan bahawa graphene satu lapisan dan dua lapisan yang simetrik menunjukkan jurang jalur kosong, manakala graphene dwi-lapisan yang simetrik memberikan jurang jalur 0.35 eV. Pembukaan jurang jalur bagi graphene dwi- dan banyak lapisan yang simetrik adalah terhad dan menurunkan kelincahan elektron. Jadi pendekatan lain untuk membukakan jurang jalur tanpa merosakkan kelincahan elektron yang tinggi dalam graphene satu lapisan, adalah dengan mendopkan graphene. Kerja ini telah menunjukkan bahawa kemasukan atom-atom dopan dalam graphene satu lapisan menghasikan peningkatan dalam jurang jalur, dengan penambahan bilangan atom pendopan. Kedudukan atom-atom pendopan dalam graphene satu lapisan juga memberi kesan signifikan terhadap pembukaan jurang jalur. Didapati bahawa atom-atom oksigen dalam graphene menghasikan pembukaan jurang jalur yang lebih tinggi berbanding atom-atom boron. Keupayaan untuk mengubah jurang jalur graphene satu lapisan ini boleh digunakan untuk banyak aplikasi-aplikasi dalam elektronik digit. Untuk aplikasi analog, penyelidikan ini memfokuskan kepada penyiasatan kesan panjang saluran dan ketebalan get oksida bagi transistor graphene kesan medan (GFET). Fabrikasi GFET ini memerlukan liputan graphene satu lapisan yang baik. Kerja ini telah menjalankan pengoptimuman dalam proses pemindahan graphene, dimana kaedah penyeteman menggunakan blok kayu telah dicadangkan. Suatu proses pencucian sampel dalam acetone juga sangat penting untuk mendapatkan lapisan graphene yang baik sebelum GFET boleh difabrikasikan. Dalam kerja ini, prestasi GFET telah disiasat berdasarkan kelincahan cas pembawa diambil daripada kedua-dua pengangkutan electron dan lohong, GFET telah difabrikasikan dengan dua get oksida pada ketebalan 63 dan 83 nm dengan panjang saluranberbeza daripada 250 μm ke 650 μm . Keputusan-keputusan menunjukkan bahawa kelincahan elektron dalam GFET meningkat apabila panjang saluran menurun. Corak yang sama dicerap untuk kelincahan pembawa lohong. Bagaimanapun, didapati bahawa kelincahan elektron dan lohong menurun apabila ketebalan get oksida meningkat. Boleh disimpulkan bahawa panjang saluran dan ketebalan get oksida GFET memainkan peranan penting dalam mendapatkan prestasi GFET, dimana laju suatu peranti bertambah dengan saluran yang lebih pendek dan get oksida yang lebih tebal.

Simulation of Graphene Band Structure and Fabrication of Graphene Field Effect Transistor

ABSTRACT

This thesis presents an approach in exploring graphene for digital electronics, as well as analogues. For digital electronic application, this work focused on opening and tuning the monolayer graphene band gap based on the inclusion of dopant atoms, by using AtomixKit Simulator from Quantum Wise. Two sets of simulation have been carried out, that are, to study the graphene band structures based on the effect of asymmetrical bilayer graphene layers and doping the monolayer graphene with boron and Oxygen atoms. Results have shown that monolayer and symmetrical bilayer graphene exhibit zero band gaps, while asymmetrical bilayer graphene provides a band gap of 0.35 eV. The opening of energy band gap in asymmetrical bi- and multi-layer graphene is limited and reduces electron mobility. So another approach to open the band gap without disrupting the high electron mobility in monolayer graphene, is by doping the graphene. This work has shown that the inclusion of dopant atoms in monolayer graphene results in an increase in the band gap, with increased number of dopant atoms. The position of the dopant atoms in monolayer graphene also significantly affects the band gap opening. It is obtained that Oxygen atoms in graphene give rise to higher band gap openings compared to boron atoms. This ability to modify the monolayer graphene band gap can be applied for many digital electronic applications. For analogue application, this research focused on investigating the effect of channel length and gate oxide thickness of graphene field effect transistor (GFET). This GFET fabrication required a good coverage of monolayer graphene. This work has performed an optimization in the graphene transfer process, in which a stamping method using a wooden block is suggested. A proper cleaning process in acetone is also crucial in order to obtain a good layer of graphene before GFET can be fabricated. In this work, the GFET performance is investigated based on the charge carrier mobility taken from both transportation of electrons and holes. The GFETs have been fabricated with two different gate oxides with thicknesses of 63 nm and 83 nm with channel lengths varied from 250 μm to 650 μm . Results have shown that the electron mobility in GFET increases as the channel lengths decreases. The same pattern is observed for hole carrier mobility. However, it is obtained that the electrons and holes mobility decreases as the gate oxide thickness increases. It can be concluded that the GFET channel length and gate oxide thickness play an important role in determining the GFET performance, as the speed of the device increases with shorter channel and thicker gate oxide.

CHAPTER 1

INTRODUCTION

1.1 Overview of Graphene

Graphene was discovered by two physicists from Manchester University in 2004 (Novoselov et al., 2004) and since then graphene has become popular in research and applications (Yue et al., 2015, Arefinia et al 2015, Hsieh et al 2015 and Tan. et al., 2015) due to its remarkable electronic and mechanical properties. Currently, many applications using graphene as the base material has been explore. This makes graphene suitable to be use in electronics applications (Lie et al., 2015, Valentini, 2015, Ramachandran et al., 2015, Veronose G. et al., 2015, Luo et al. 2015 and Sreejesh et al., 2015).

Graphene carrier mobility of between 3000 to 60000 cm^2/Vs was reported in 2004 (Geim et al., 2004), thus makes graphene as a promising material for future nano electronic devices. Soon in 2008, a carrier mobility of up to 200 000 cm^2/Vs was recorded for graphene (Kwon K. et al 2015). Graphene also reported having a much higher conductivity of 1097 Scm^{-1} than other carbon materials and a very good flexibility material with only < 5% loss of electrical conductivity (Bolotin K. et al., 2008). Besides that, graphene is also reported to have sheet resistance of $\sim 10^{-6} \Omega\text{cm}$ which is less than the resistivity of silver, which is known to have the lowest resistivity at room temperature (University of Maryland,

2008). With this remarkable features, graphene has been studied and applied in many applications such as RF devices, sensing devices, flexible electronics and many more.

1.2 Problem Statement

Even though graphene promises many excellent properties which make it promising in replacing silicon in digital electronic and analogue application, however, to incorporate it into a device, a lot of issue emerges. In digital electronic for instance, graphene face a major issue due to its gapless energy band. This is because in digital electronic, band gap is needed so that a device can be turned on and off. Contradict to this situation; graphene will put the device in on state all the time.

Realizing this issue, many researches had been carried out in order to open a band gap in graphene. A research by Zhang et al., 2009 and Khodkov et al., 2012 proposed opening a band gap in graphene by increasing the numbers of graphene layer. This method succeeded in opening the band gap, however the band gap increment is limited due to charged impurity scattering, thus making it not suitable for certain application such as power devices and radio frequency (RF) devices which requires band gap larger than 2 eV (Brillson, 2010). There is also a method such as applying uniaxial strain to graphene sheet in order to widen the graphene band gap (Ni et al., 2009). However this method requires a very strong strain which is quite difficult to carry out in order to suit the device specification.

Another method proposed to open graphene band gap is by applying external electric to bilayer graphene (McCann, 2006; Castro et al., 2007; Oostinga et al., 2008). This method also has succeeded in opening the band gap; however the carrier mobility in bilayer graphene becomes smaller than monolayer graphene. Carrier mobility is one of the main interests in graphene; therefore sustaining its high mobility had been a great deal. Fujita et al., 1996, Nakada et al., 1996 and Son et al., 2006 proposed to modify the graphene sheet with dominant edge structures like nanoribbons in order to open monolayer graphene band gap. However it is difficult to precisely tune the band gap magnitude by using this method because the edge structure is difficult to control. Therefore, another method which can significantly control the bandgap tuning is by doping the monolayer graphene with heteroatom like sulfur, aluminium, silicon and phosphorus (Pablo, 2010). This method is able to maintain the high carrier mobility in monolayer graphene with controllable band gap opening.

This research is focused on opening the monolayer graphene band gap with hetero atoms; boron and oxygen atoms as the dopants. Boron and oxygen were chosen due to their atom size which are slightly different than the carbon atom, in which a carbon has atomic radius of 70 pm, however a boron has atomic radius of 85 pm and an oxygen is 60 pm. Boron is also chosen in this study due to its 3 valence electrons, and oxygen has 6 valence electrons. Since a carbon atom has 4 valence electrons, carbon-boron and carbon-oxygen bonding make good covalent bonds. These two different dopant atoms in graphene sheet were studied based on their effects to the graphene band structure and subsequently, to graphene electronic properties. However, in this work the opening of band gap in

monolayer is done by using simulation. Simulation work gives an advantage to this research in providing a controlled environment so that a basic principle of ideal condition (without the existence of impurities) of doped monolayer graphene can be studied. Furthermore the concentration of dopants can also be systematically controlled by using simulation that eventually leads to proper analytical analysis.

As for analogue application, one of the most common issues regarding the application of graphene is to incorporate graphene in electronic devices. This work focused on the fabrication of graphene field effect transistor (GFET), where graphene is incorporated as the channel material, replacing inversion layer that is formed in typical field effect transistor (FET). Based on graphene excellent electronic properties, the graphene layer will form a uniform inversion layer with controlled electron conduction. So, it is expected that GFET operates similarly to a typical FET devices. Hence, this work investigates the effect of graphene layer as the channel material in GFET based on the device performance over typical FET.

Even though graphene is known to have high carrier mobility, but using graphene as a channel material in FET is a challenge. There are a few limitations in the fabrication of devices with the inclusion of graphene that have been reported. One of it is the quality of the contact between graphene and electrodes (Nagashio et al., 2010; Khomyakov et al., 2010). This issue has a significant effect on the electronic transport of the device. A high contact resistivity will affect the total of on state current, hence the transistor performance. It will also negatively influence the peak trans-conductance and the linearity of the current versus gate-voltage characteristics (Parish et al., 2011).

Even though previous research have promised a solution to each issue that are identified regarding the performance of GFETs, there is still no commercialized GFET from the semiconductor industry due to its high fabrication cost. Therefore this research focused on using methodology and material that requires less complex process and cheap, with an aim of elevating the performance of typical Si FET devices.

Other than the inclusion of graphene layer in the GFET, the overall design of GFET are fine tuned in order to ensure the device design and performance are pulled together. In accordance to that, the metal contact for the GFET is using aluminium, in which it is chosen to replace gold that has been used in previous research (Vasiri, 2011). Even though gold is known to have very high conductivity, however its cost is high, therefore aluminium is chosen. Regardless the fact that aluminum is cheaper than gold, aluminum still offers high conductivity and strong adhesion to the substrate.

Besides that, this work implemented a top gated GFET design, which is aimed to eliminate the parasitic capacitance that exist in back gated transistor. This research also has chosen silicon dioxide (SiO_2) as the dielectric material replacing the high K dielectric (high dielectric constant) material that has been widely used in the fabrication of GFET.

1.3 Research Objectives

- i. To investigate the graphene band gap opening based on graphene doped with different dopant atoms.

- ii. To investigate the effect of different channel lengths and different gate oxide thickness to the performance of GFETs.
- iii. To design and fabricate a low cost, feasible GFETs with reasonable performance.

1.4 Research Scope.

This research focuses on two main topics which are the simulation of graphene and the fabrication of GFETs. The simulation of graphene focused on investigating the band structure that involves initial investigation on opening the graphene band gap based on different number of graphene layers; monolayer, bi-layer and multi-layer graphene. However, the opening of the band gap is limited and reduced the carrier mobility in graphene. Hence the simulation later is done focusing on monolayer graphene to sustain its carrier mobility, while the band gap opening is in better control. However a careful investigation need to be made to ensure the effect of the dopant atoms are significant in the band opening. As for the fabrication of GFET, this work used graphene that has coverage of ~70% monolayer graphene and ~30% bi- and multi-layer graphene.

Doped graphene is difficult to be incorporated in the GFET due to the newly developed graphene transfer process which would incorporate additional defects in the doped graphene. However, the inclusion of doped graphene in GFETs is proposed for the continuation of this project and its discussion is included in chapter 5. In the GFET

fabrication, two main parameters are investigated, that are, the channel lengths and gate oxide thickness. In the completion of the GFET fabrication, the graphene transfer process, GFET design, and characterizations are involved and will be presented in this thesis.

1.5 Thesis Outline

This thesis consists of five chapters which are Introduction, Research Background, Methodology, Results and Discussion and last but not the least, Conclusion. This thesis outline is given below:

Chapter 2: Research Background

This chapter presents graphene from fundamental point of view, in which the discussion is given based on graphene physical and electronic properties, and particularly on its energy band structure. The preparation of graphene layers is also presented. This chapter also presents an overview of GFET technology and development.

Chapter 3: Methodology

This chapter explains both simulation and fabrication processes that are carried out in this work. For the simulation part, the software is presented based on the graphene structure development, followed with extraction of the graphene band structure. For the GFET, the

fabrication process, graphene transfer process and characterization using AFM, optical microscope and point probes are presented.

Chapter 4: Results and Discussion

This chapter presented the results obtained from the simulation of graphene followed with results from the characterization of GFET. All the results are discussed and analyses are carefully made.

Chapter 5: Conclusion and Future Work

This chapter concludes the finding for both simulation of graphene and fabrication of GFET. This chapter also proposed the possible future works that can be done, initiated from this research.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter begins with discussion on graphene that covers the structure of graphene, tight binding model and preparation of graphene. Next the issue regarding to the opening of graphene band gap is reviewed. This chapter also explains previous methods that had been carried out in order to open the band gap of graphene. Subsequently this chapter continues with the discussion of graphene transfer processes. In the end of this chapter the graphene field effect transistor (GFET) that includes the designs and characterization of the device will be presented.

2.2 Graphene

This section covers basic understanding on graphene that comprises of the topic of physical properties of graphene, energy dispersion and the preparation of graphene. Further details regarding to these topics will be explained in the next section.

2.2.1 Physical Properties of Graphene and Energy Dispersion

Graphene is a two dimensional (2D) material and is an allotrope of carbon. Carbon atoms in graphene are densely packed in a regular atomic-scale chicken wire (hexagonal) pattern as shown in Figure 2.1. As shown in the figure, lattice in graphene sheet has two fundamental carbon atoms denoted as atom 1 and atom 2, which are the basic elements of the whole lattice to form a unit cell. Thus, the lattice of unit cells is periodic.

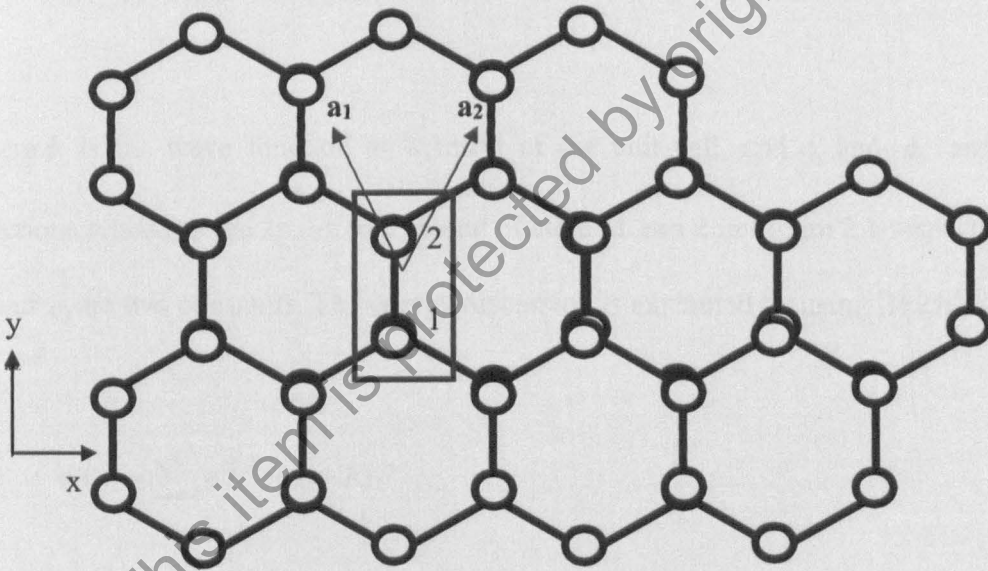


Figure 2.1 Hexagonal pattern of graphene

Each point on the periodic lattice in Figure 2.1 can be derived as $\vec{R} = m\vec{a}_1 + n\vec{a}_2$

where m and n are two integers and a_1 and a_2 are two unit vectors that are defined as